EXHIBIT A

Technical Brief
SWRA029

Fractional/Integer-N PLL Basics

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Abstract

Phase Locked Loop (PLL) is a fundamental part of radio, wireless and telecommunication technology. The goal of this document is to review the theory, design and analysis of PLL circuits. PLL is a simple negative feedback architecture that allows economic multiplication of crystal frequencies by large variable numbers. By studying the loop components and their reaction to various noise sources, we will show that PLL is uniquely suited for generation of stable, low noise tunable RF signals for radio, timing and wireless applications.

Some of the main challenges fulfilled by PLL technology are economy in size, power and cost while maintaining good spectral purity.

This document details basic loop transfer functions, loop dynamics, noise sources and their effect on signal noise profile, phase noise theory, loop components (VCO, crystal oscillators, dividers and phase detectors) and principles of integer-N and fractional-N technology. The approach will be mainly heuristic, with many design examples.

This document is written for designers, technicians and project managers. Design procedures, equations, performance interpretation, CAD and examples are included to help those who have little experience. A list of reference books and articles is also included.

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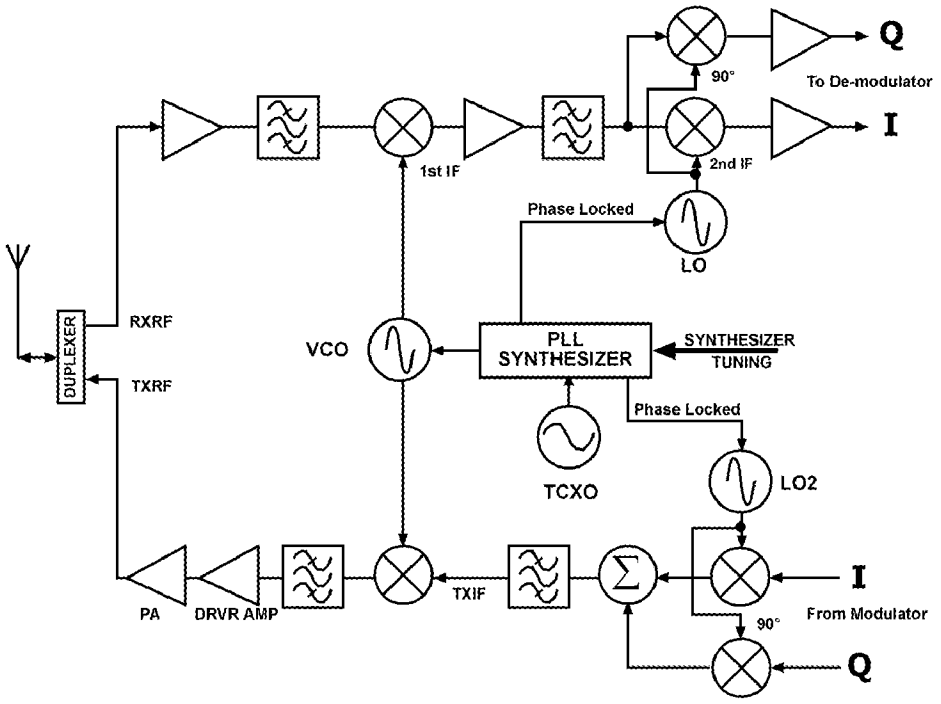
Introduction to Phase Locked Loop (PLL)

Until DSP technology is capable of directly processing and generating the RF signals used to transmit wireless data, traditional RF engineering will remain a fundamental part of wireless communication systems design. As it stands, wireless transceivers must still be able to generate a wide range of frequencies in order to upconvert the outgoing data for transmission and downconvert the received signal for processing (see Figure 1).

Figure 1. General Transceiver Block Diagram



Although there are a variety of frequency synthesis techniques, phase locked loop (PLL) represents the dominant method in the wireless communications industry. PLL, like most wireless communication technologies, is relatively new and has matured only in the last decade. The ability to execute all PLL functions on a single integrated circuit (IC) has created an economical, mass production solution to meet the needs of industry. Current PLL ICs are highly integrated digital and mixed signal circuits that operate on low supply voltages and consume very low power. These ICs require only an external crystal (Xtal) reference, voltage controlled oscillators (VCO), and minimal external passive components to generate the wide range of frequencies needed in a modern communications transceiver. Although a proven technology, PLL is still changing and evolving to keep pace with the wireless revolution.

The problems associated with operating a wireless communications system have become especially acute in the last few years with the advance of cellular telephony and the emergence of wireless data networks. Because there are more users now, most operating at progressively higher data rates, both interference and signal-to-noise-ratio have become key considerations in system design. Phase noise and spurious emissions contribute significantly to both of these issues and are largely dependent on the performance of the PLL IC. Minimizing phase noise and spurs of the frequency synthesizer while staying within power consumption, size, and cost restraints is one of the challenges for today's RF design engineers. We will see later how an emerging PLL technology called fractional-N synthesis has made this task more manageable.

The purpose of this document is to illustrate practical PLL signal generation techniques, review PLL basic building blocks, explain various phase noise sources and their measurement, and compare integer-N and fractional-N PLL technologies. The focus will be on basic principles, synthesis parameters, phase noise and its measurement, as well as design trade-off. This document is intended for design, system, and test engineers as well as technicians and technical managers.

Frequency Synthesis

Frequency Synthesis is the engineering discipline dealing with the generation of multiple signal frequencies, all derived from a common reference or time base. The time base used is typically a Temperature Compensated Crystal Oscillator (TCXO). The TCXO provides a reference frequency to the synthesizer circuit so that it may accurately produce a wide range of signals that are stable and relatively low in phase noise.

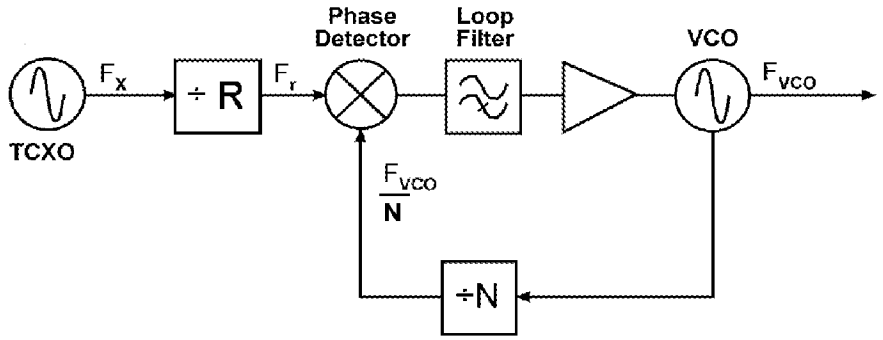
Digital PLL Synthesis

Among the many different frequency synthesis techniques, the dominant method used in the wireless communications industry is the digital PLL circuit. While there are some benefits to using other synthesis techniques, they are outside the scope of this document and will not be discussed here.

Integer-N PLL

Compared to the analog techniques used in the infancy of frequency synthesis, the modern PLL is now a mostly digital circuit. Figure 2 shows a typical block diagram of a PLL implemented with a TCXO reference.

Figure 2. Integer-N (classical) PLL Block Diagram



This traditional digital PLL implementation will be termed "integer-N" to avoid confusion due to the addition of fractional-N technology. The PLL circuit performs frequency multiplication, via a negative feedback mechanism, to generate the output frequency, Fvco, in terms of the phase detector comparison frequency, Fr.

$$Fvco = N \bullet Fr \quad \text{(Equation 1)}$$

To accomplish this, a reference frequency must be provided to the phase detector. Typically, the TCXO frequency (Fx), is divided down (by R) "on-board" the PLL IC. The phase detector utilizes this signal as a reference to tune the VCO and, in a "locked state," it must be equal to the desired output frequency, Fvco, divided by N.

$$Fvco / N = Fx / R = Fr \quad \text{(Equation 2)}$$

Thus, the output frequency that the synthesizer generates, Fvco, can be changed by reprogramming the divider N to a new value. By changing the value N, the VCO can be tuned across the frequency band of interest. The only constraint to the frequency output of the system is that the minimum frequency resolution, or minimum channel spacing, is equal to Fr.

$$Channel\ spacing = Fvco / N = Fr \quad \text{(Equation 3)}$$

When the PLL is in unlocked state (such as during initial power up or immediately after reprogramming a new value for N) the phase detector will create an error voltage based on the phase difference of the two input signals. This error voltage will change the output frequency of the VCO so that it satisfies Equation 2. As long as the system is in a locked condition the VCO will have the same frequency accuracy as the TCXO reference. If the crystal accuracy is 1 part-per-million (ppm), the output frequency of the synthesizer will also be accurate to 1 ppm.

Specifically, if Fr = 30 kHz and N = 32000, the only way for this circuit to be in a stable state (locked) is when Fvco = 960 MHz. If N were changed to 32001, a frequency and phase error will develop at the input of the phase detector that will, in turn, retune the VCO frequency until a locked state has been reached. The locked state will be reached when Fvco = 960.03 MHz and, if the TCXO has an accuracy of 1ppm, the output of the VCO will be accurate to ~ +/- 960 Hz.

Fractional-N PLL

An unavoidable occurrence in digital PLL synthesis is that frequency multiplication (by N), raises the signal's phase noise by 20Log(N) dB. The main source of this noise is the noise characteristics of the phase detector's active circuitry. Because the phase detectors are typically the dominant source of close-in phase noise, N becomes a limiting factor when determining the lowest possible phase noise performance of the output signal. A multiplication factor of N = 30,000 will add about 90 dB to the phase detector noise floor. 30,000 is a typical N value used by an integer PLL synthesizer for a cellular transceiver with 30 kHz channel spacing. It would seem that we could radically reduce the close-in phase noise of our system by reducing the value of N but unfortunately the channel spacing of an integer-N synthesizer is dependent on the value of N (see Equation 3.) Due to this dependence, the phase detectors typically operate at a frequency equal to the channel spacing of the communication system.

A phase detector is a digital circuit that generates high levels of transient noise at its frequency of operation, Fr. This noise is superimposed on the control voltage to the VCO and modulates the VCO RF output accordingly. This interference can be seen as spurious signals at offsets of +/- Fr (and its harmonics) around Fvco. To prevent this unwanted spurious noise, a filter at the output of the charge pumps (called the loop filter) must be present and appropriately narrow in bandwidth. Unfortunately, as the loop filter bandwidth decreases, the time required for the synthesizer to switch between channels increases.

For a 2^{nd} order loop with natural frequency (loop bandwidth) ωn and damping factor ξ, the switching speed (Tsw) is proportional to the inverse of their product.

$$Tsw \propto 1/\omega n\xi \qquad \text{(Equation 4)}$$

If N could be made much smaller, Fr would increase and the loop filter bandwidth required to attenuate the reference spurs could be made large enough so that it does not impact the required switching speed of our system. Once again, however, the upper limit of Fr is bound by our channel spacing requirements. This illustrates how our desires to optimize both switching speed and spur suppression directly conflict with each other.

A newly emerging PLL technology has made it possible to alter the relationship between N, Fr, and the channel spacing of the synthesizer. It is now possible to achieve frequency resolution that is a fractional portion of the phase detector frequency. This is accomplished by adding internal circuitry that enables the value of N to change dynamically during the locked state. If the value of the divider is "switched" between N and N+1 in the correct proportion, an average division ratio can be realized that is N plus some arbitrary fraction, K/F. This allows the phase detectors to run at a frequency that is higher than the synthesizer channel spacing.

$$Fvco = Fr\,(N + K / F)\ N, K, F \text{ are integers} \qquad \text{(Equation 5)}$$

Where: F = The fractional modulus of the circuit (i.e. 8 would indicate a $1/8^{th}$ fractional resolution.)
K = The fractional channel of operation.

PLL Parameters

There are several important parameters for signals generated by a PLL circuit.

Frequency range, or tuning bandwidth - the frequency band needed for the application. Most cellular, PCS and Satcom applications are narrow band (covering 3-10% bandwidth.) As an example North American cellular standards, AMPS, TDMA or CDMA, cover 25 MHz in the 900 MHz band.

Step size or frequency resolution - the smallest frequency increment possible. It is Fr for integer-N and Fr/F for fractional-N. In the North American cellular system, step size is 30 kHz. In China, Japan and the Far East it is 25 kHz. In Europe, the GSM cellular system requires a 200 kHz step. In FM broadcasting radio, the step size is 100 kHz.

Phase noise - an indicator of the signal quality. Phase noise and jitter are manifestations of the same phenomena (the former in the frequency domain, the later in time domain.) Clean signals have low jitter, which results in much of their total energy being "concentrated" close to the center frequency of operation. Phase noise is specified in a variety of ways: time jitter (nsec rms), degrees rms, FM noise (Hz rms) or spectral distribution density L(fm).

Spurious signal level - a measure of the discrete, deterministic, periodic interference "noise" in the signal spectrum. Spurious signals are part of the signal's "noise spectrum" and represent any discrete spectral line not related to the signal itself. Harmonics (and sometimes sub-harmonics) are usually not considered as spurious signals and are dealt with separately.

Loop bandwidth - a measure of the dynamic speed of the feedback loop. Since the PLL acts as a narrow-band tracking filter, this parameter indicates this filter's single sideband bandwidth. For many designers, this bandwidth is synonymous with the loop's natural frequency $\omega n/2\pi$ or the frequency in which the open loop gain equals 1. ωn is always a design parameter when optimizing for phase noise, switching speed, or spur suppression.

Switching speed - a measure of the time it takes the PLL circuit to re-tune the VCO from one frequency to another. This parameter usually depends on the size of the frequency step. Because the synthesizer output frequency approaches the intended frequency asymptotically, switching speed is typically measured by the time it takes to settle to within a specified tolerance from the final frequency.

Other parameters deal with size, power, supply voltage, interface protocol, temperature range and reliability. A detailed discussion of these parameters is beyond the scope of this document.

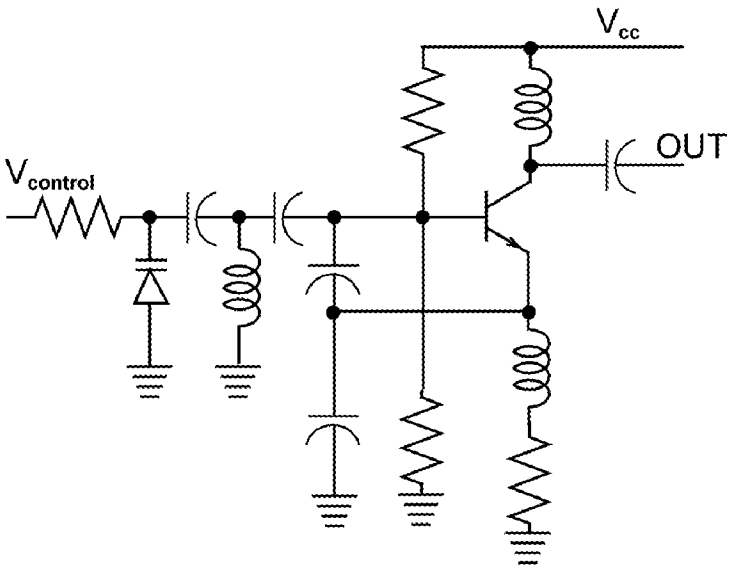
PLL Components

The four basic components of a PLL circuit are the VCO, the phase-frequency detector, the main and reference dividers, and the loop filter. Typically, the PLL IC integrates the dividers and phase detectors onboard. The reason for excluding the VCO and loop filter is to prevent the noise associated with the digital dividers and phase detectors from coupling with the VCO's active circuitry. This also allows the IC more flexibility in application.

Voltage Controlled Oscillators (VCO)

The VCO generates the output signal from the synthesizer. Voltage controlled oscillators are positive feedback amplifiers that have a tuned resonator in the feedback loop. Oscillations occur at the resonant frequency, which is typically changed, or tuned, by varying the resonator capacitance. VCOs are oscillators whose resonant tank circuit can be tuned via a control voltage that is applied across a varactor in the tank circuit. In the cellular and PCS bands, most VCOs are "negative resistance" types, with a resonator in the transistor base or emitter. Though different designers have their own schemes, they are quite similar in structure. Figure 3 shows a typical VCO design example.

Figure 3. L-Band VCO Schematics



The theoretical transfer function of a VCO is given by $ks/(s^2+\omega o^2)$. In practice, the Q of the resonator must be finite and the transfer function poles will be slightly to the left of the imaginary axis on the complex plane (poles to the right or on the imaginary axis would yield a signal with infinite energy, which is not achievable).

Varying the DC voltage across the varactor diode, which is part of the tank circuit, controls the VCO frequency. The inductor and the varactor both limit the Q of the tank circuit.

Table 1. Typical Q for Inductors and Varactors in the 800-2000 MHz Range

Type of component	Typical Q
Microstrip line on Fr-4	6-12
Air-coil	20-50
Ceramic materials	50-200
Saw resonator	400-2000
Varactor (2-6 pF)	40-100

A VCO can be specified by its tuning gain, Kv. This is the amount of frequency deviation (in MHz) that results from a 1-volt change in the control voltage. It is measured in units of MegaHertz per Volt (MHz/V). The noise level on the VCO control line is determined by active devices and is not typically variable in a given application. Therefore, a lower Kv will generate a lower phase noise. For example, 1 μV of noise on the control line will generate 20 Hz FM noise for Kv = 20 but only 2 Hz FM noise for Kv = 2. Typically, if we raise the Q of the tank circuit, we will improve the phase noise characteristics by reducing Kv (and ultimately the tuning bandwidth) of the VCO. Kv linearity is also very important because of its effect on loop dynamics. As we will see ahead in Equation 8, Kv directly affects the loop transfer function, and therefore its bandwidth. A nonlinear change in Kv across the frequency band of interest will have an affect on loop bandwidth, phase noise, and switching speed that cannot be easily accounted for by the system designer.

Oscillator design can be accomplished by analyzing either the open loop transfer functions, or the closed loop s-parameters. In the open loop analysis, oscillation will occur at the frequency where the open loop phase shift is 360 degrees and the open loop gain is greater than 1 (see Figure 4 and Figure 5).

Figure 4. Oscillator Open Loop Gain Model

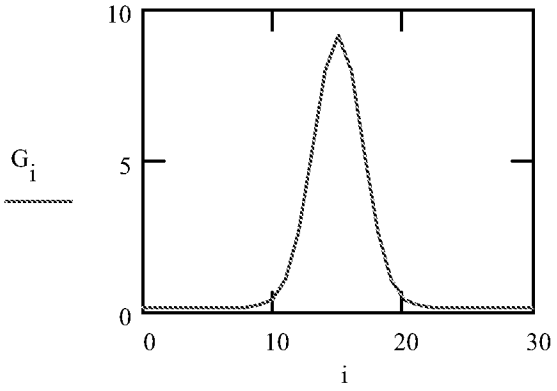
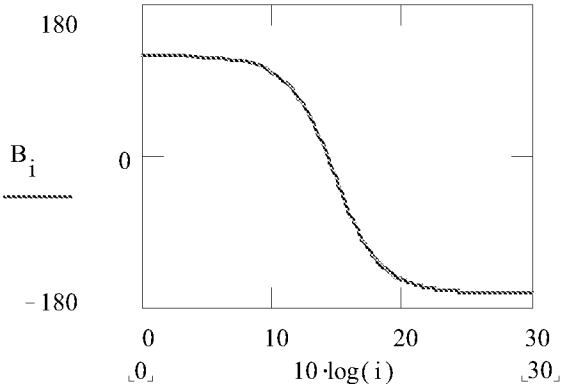


Figure 5. Oscillator Open Loop Phase Model



A VCO will start to oscillate as a consequence of background noise in the circuit. This background noise is due to the noise figure of the amplifier, the resistors, and the finite Q of the resonator. When the VCO is initially powered up, noise that is present within the frequency band of the resonator is amplified until the circuit reaches saturation. When the amplifier reaches saturation, the amplitude of the noise will stabilize and the oscillator will reach a steady state condition. If G(s) is the VCO transfer function, then the output spectrum will be given by:

$$S_0(f) = F \bullet kT \bullet |G(s)|^2 \qquad \text{(Equation 6)}$$

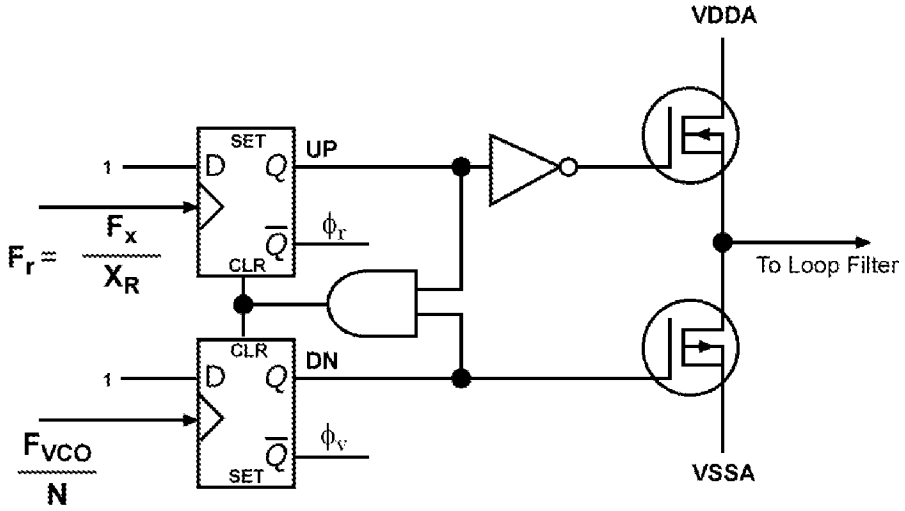
Where: k is Boltzman's constant
T is the ambient temperature in degrees Kelvin
F is the total noise figure.

The output spectrum of a VCO is therefore composed of bandpass amplified noise. The loaded Q of the resonator determines the "quality" of this noise (that is, how "narrow band" this noise is). For convenience, we model this noise signal as a sinusoid plus some arbitrary amount of noise. Almost all models use the Leeson approximation.

Phase Frequency Detectors (PFD)

The phase detector generates the error signal required in the feedback loop of the synthesizer. The majority of PLL ASICs use a circuit called a Phase Frequency Detector (PFD) similar to the one shown in Figure 6. Compared with mixers or XOR gates, which can only resolve phase differences in the +/- π range, the PFD can resolve phase differences in the +/- 2π range or more (typically "frequency difference" is used to describe a phase difference of more than 2π, hence the term "phase frequency detector." This circuit shortens transient switching times and performs the function in a simple and elegant digital circuit.

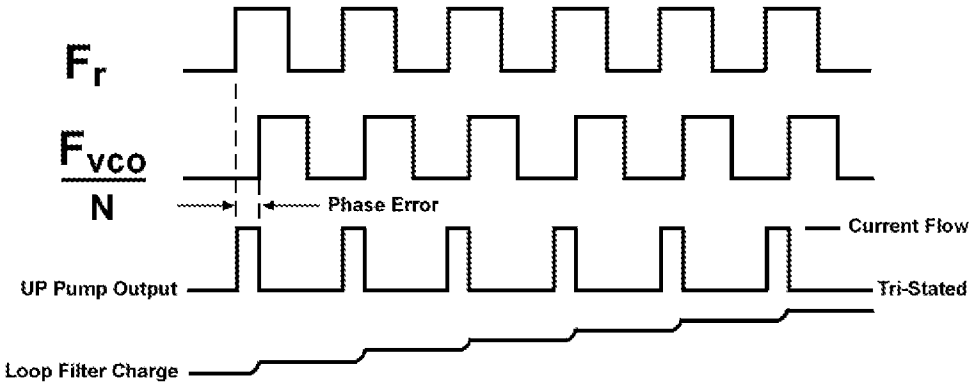
Figure 6. Phase Frequency Detector Schematic



The PFD compares the reference signal Fr with that of the divided down VCO signal (Fvco/N) and activates the charge pumps based on the difference in phase between these two signals. The operational characteristics of the phase detector circuitry can be broken down into three modes: frequency detect, phase detect, and phase locked mode. When the phase difference is greater than $\pm 2\pi$, the device is considered to be in frequency detect mode. In frequency detect mode the output of the charge pump will be a constant current (sink or source, depending on which signal is higher in frequency.) The loop filter integrates this current and the result is a continuously changing control voltage applied to the VCO. The PFD will continue to operate in this mode until the phase error between the two input signals drops below 2π.

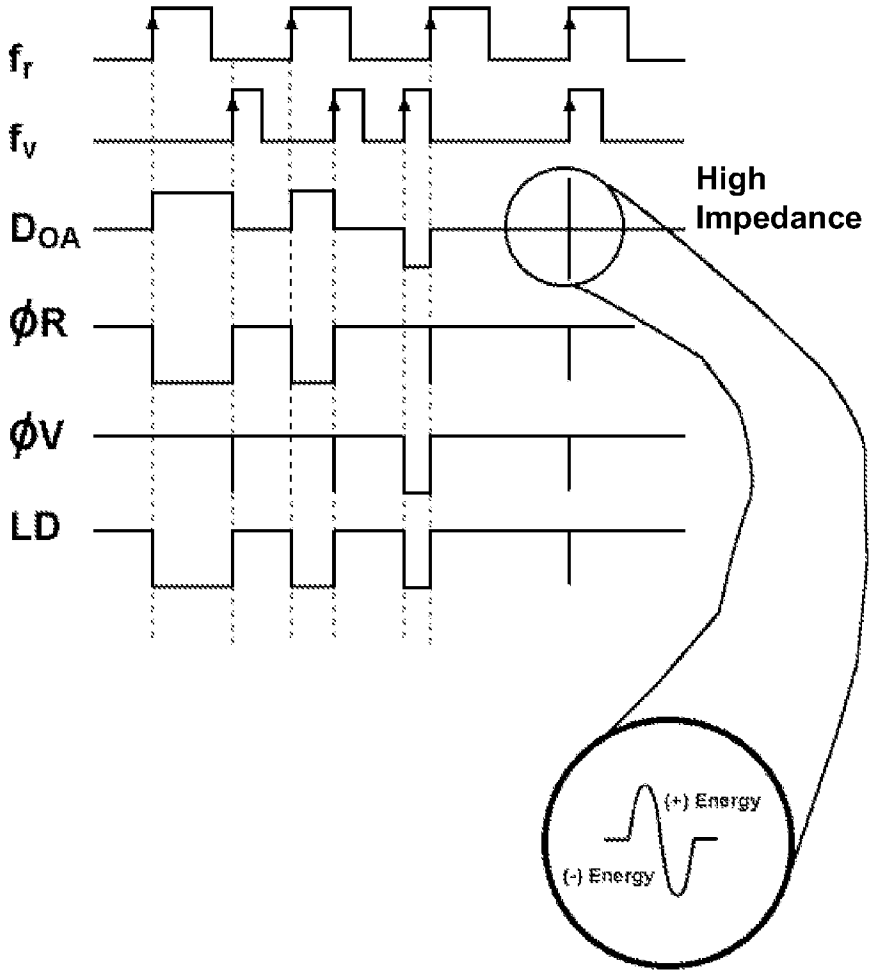
Once the phase difference between the two signals is less than 2π, the PFD begins to operate in the phase detect mode. In phase detect mode the charge pump is only active for a portion of each phase detector cycle that is proportional to the phase difference between the two signals (see Figure 7). Once the phase difference between the two signals reaches zero, the device enters the phase locked state (see Figure 8.)

Figure 7. Phase Detector Output (Voltage, Current) Waveforms, for Fv/N<Fr



In the phase locked state, the PFD output will be narrow “spikes” that occur at a frequency equal to Fr. These current spikes are due to the finite speed of the logic circuits (see Figure 8, D_{OA} blowup) and will have to be filtered so they do not modulate the VCO and generate spurious signals.

Figure 8. Phase Detector Timing Waveforms



Dividers

Dividers constitute a main function in PLL circuits. A PLL circuit needs to cover a very wide range of continuous divisions for the crystal reference and for the VCO (see Figure 2). Two types of dividers are used, high speed and low speed.

High Speed Dividers

For the high-frequency VCO's (200-2500 MHz), dual modulus dividers are employed to achieve a simple continuous division mechanism. For example, an AMPS phone needs to cover 25 MHz with 30 kHz steps. This requires the generation of about 850 contiguous N values

A "P / P+1" dual modulus divider will divide by either P or P+1 based upon external command. It has a Modulus Control (MC) input port (typically TTL or CMOS) controlling the number of times to divide by P or P+1. The lowest contiguous divide ratio for a dual modulus device is given by $P^2 - P$. Specifically, a 16/17 divider allows generation of contiguous divider values above N = 239.

Example

A divide values of N = 960 is accomplished by dividing the input signal by 16 a total of 60 consecutive times. Changing N to 961 requires that we divide the signal by 16 a total of 59 times and then divide the signal by 17 once, and so on. If we need to generate divisions in the 100-150 range using a 16/17 device there will be some numbers that can not be generated. A divide ratio of 100 can be gained by dividing twice by 16 and 4 times by 17 (17 * 4 + 16 * 2 = 100). However, there is no combination of 16 and 17 that can generate the number 103. To generate contiguous division numbers in this range would require a lower dual modulus (8/9, 10/11, etc). Dual modulus devices typically employ bipolar technology due to current consumption and speed requirements.

To run high division numbers and allow lower divisions (lower than P^2-P), tri-modulus and even quad-modulus circuits are used. One common configuration, 64/65/72, is used in a few PLL chips. For a tri-modulus P/(P+1)/(P+R) divider, the minimum continuous divide number, Nmin, is given by:

$$Nmin = (P/R + R + 1) * P + R \qquad \text{(Equation 7)}$$

For a 64/65/72 divider Nmin = 1096, compared with Nmin = 4032 for a 64/65 divider.

Low Speed Dividers

The second type of divider is the regular programmable counter. These counters typically use CMOS technology, run at frequencies up to 100 MHz, and consume very low power. These counters are used as the reference divider and also as dual modulus control counters.

A complete PLL "N" divider is typically implemented using a dual modulus divider controlled by two programmable counters, usually described as the "A counter" which determines the number of times the input is divided by P+1 and the "M counter" which determines the number of times the input is divided by P.

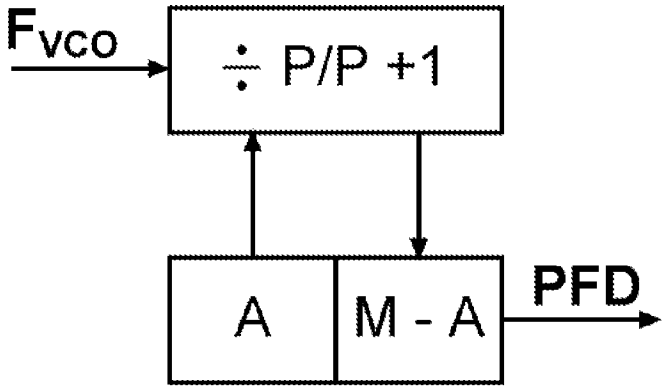
The total division ratio for the divider is given by:

$N = P \bullet A + (P+1) \bullet (M-A)$.

Note that when A is incremented by 1, M-A decreases by 1 and the total division ratio, N, increases by 1.

Note also that the minimum required bit size of the A counter is equal to the bit size of P. For 64/65, the A counter has to be of no more than 6 bits ($64=2^6$). A block diagram of a programmable divider using a dual modulus divider is shown in Figure 9.

Figure 9. Programmable Divider Using Dual Modulus



Loop Filter

There are two types of loop filters, active and passive. Active loops use op-amps, are usually differential, and allow the synthesizer to generate tuning voltage levels higher than the PLL IC can generate on-chip. The op-amp itself provides the DC amplification necessary to develop a control voltage that is higher than the on-chip supply of the phase detector. Active loops are used in wide band applications that require wide DC voltages to control the VCO. Passive filters are mainly R, C (resistor, capacitor) elements that connect directly between the PLL ASIC and VCO. Most PLL ASICs use a current source for the output to generate the control voltage. This output is proportional to the phase error (for example: +/- 1mA for +/- 2π phase error). This " current source" loop filter configuration is the most popular for wireless, narrow-band applications (see Figure 15).

The Simple Math of PLL

In this section, we present a short review of basic feedback loop principles and theory, and develop transfer functions to study the effect of various noise sources on output noise. But first we must state a most important synthesis principle: "multiplication of a given frequency by N increases the signal's phase noise by N or 20log(N)." Division, conversely, reduces the phase noise by this same factor. This effect can impact the communications system drastically. In the US AMPS or TDMA standard, multiplication by 30000 is required to generate signals in the 900 MHz range from a 30 kHz phase detector frequency. The signal's phase noise is therefore increased by 20log(30000) $\approx$ 90 dB. To put this in perspective, the phase noise of the RF signal (compared to the reference signal) has increased by a factor of one billion!

The following example helps the reader visualize the mechanism of this effect: suppose that a 1 MHz signal has a time jitter (noise) of 1 psec rms. When this signal is multiplied 1000 times to 1 GHz, the output jitter (assuming noiseless counters) stays at 1 psec, but the signal time period has decreased from 1μs to 1ns. Thus the period-to-jitter ratio has degraded 1000 times or 60dB.

Feedback Loop Analysis

We can now derive the loop equations by following the closed loop (Figure 2) path in the Laplace domain as follows:

Let φr represent the reference phase (Fr) and φo the output phase (Fo). We'll denote the loop filter network as H(s). Then, the output of the phase detector is given by:

$E(s) = (\varphi_r - \varphi_o/N)Kd$ Volts

$\varphi_o(s) = E(s)H(s)Kv/s$ (remember the VCO has a transfer function Kv/s)

Solving for $\varphi_{0/}\varphi_r$, (the effect of the input on the output), we get:

$$\varphi_{o/}\varphi_r(s) = \frac{KvKdH(s)/s}{1+KvKdH(s)/sN} = H1(s) \qquad \text{(Equation 8)}$$

For K = KvKd, we get H1(s) = KH(s)/[s+KH(s)/N] or

$$H1(s) = \frac{NKH(s)}{sN + KH(s)} \qquad \text{(Equation 9)}$$

Generally, from linear feedback control theory, we know that the transfer function for a specific input anywhere in the loop is given by the forward loop gain (from that input to the output point) divided by "1+ the open loop gain". The effect of different inputs (noise or modulation originating from anywhere in the circuit) can be calculated easily using these relations.

Example: If we add a signal E_ϕ after the phase detector to represent the phase detector additive noise, then we can obtain its effect on the output by noting that from this point to the output the forward gain is given by: KvH(s)/s:

$$\varphi_o/E_\phi(s) = \frac{KvH(s)}{s+KH(s)/N} = H2(s)$$

$$H2(s) = \frac{NKvH(s)}{sN + KH(s)}$$

The composite phase noise of the signal we generate with our synthesizer can be easily calculated by the sum effect of all noise sources on the output.

Another function of interest is the error function, defined by $(\varphi o-\varphi r)/\varphi r$, and given by:

$$H_E(s) = \frac{sN}{sN+KH(s)} = 1-H1(s)$$ and has a "high pass" characteristic.

Interpretation of the basic transfer function H1(s):

For low frequencies where s << KH(s)/N), H1(s) is approximately equal to N. The loop then behaves as a multiplier (by N) which is exactly what we wanted to achieve. However, when s >> KH(s)/N, the transfer function value diminishes, thus acting like a "low pass filter". Beyond a certain frequency which we describe as the loop bandwidth, the output will not follow, or track, the reference phase φ_r. We will see later that this is an advantage which allows us to shape the output noise profile. The circuit operates as a multiplier, but we can decide where we want to de-couple the output from the reference noise.

Generally, the transfer function H1(s) has a spectral shape similar to a low pass filter, multiplied by N (see Figure 10).

The error function, H_E, tells us that at low frequencies (relative to the loop bandwidth), the error will be low; the VCO will be "locked" to the reference. This is exactly what we wish since we want the VCO to acquire the stability of the reference frequency (crystal).

Overall, these transfer functions show that a PLL "locks" the VCO to the crystal (for accuracy and stability) while rejecting VCO noise close to the carrier. It does this by "shaping" the circuit noise in a low pass manner that decouples the VCO spectral profile from other noise sources.

For loop stability (an important issue in 3rd and 4th order loops), it is necessary that at the frequency where the open loop gain is unity, there will be sufficient phase margin (>45 degrees) to prevent oscillations. Phase margin is the open loop phase difference from 180 degrees (see Figure 16 and Figure 17).

The Laplace and Fourier Transform

We will use the Laplace and Fourier transformations throughout the analysis for the same reason we use them in all electronics circuits: they turn differential equations into polynomials, and allow easy interpretation of circuits and their frequency response. The Fourier transform is used for calculating steady state ($s = j\omega$) and the Laplace transform is used for transient analysis.

Fourier transform definition:

$F(\omega)=\int f(t)e^{-j\omega t}\,dt$ and the inverse:

$f(t)=\int F(\omega)e^{j\omega t}\,dt$

The integral limits are from $-\infty$ to $+\infty$.

The steady state (Fourier) response of H1(s), for H(s) = 1 (indicating no loop filter), is calculated to be: ($s = j\omega$)

$$H1(s)=\frac{K}{j\omega+K/N}$$

This is similar to a simple R/C circuit with a pole at $\omega = K/N$

Laplace transform:

$F(s) = \int f(t)\, e^{-st}\, dt$

The integral is from 0 to ∞.

Both transformations are linear.

Loop Transfer Function

Let us interpret the meaning of H1(s) of the previous section, no loop filter. The response is similar to a simple R/C circuit with a pole at $\omega = K/N$. (This is expected because we have just a single integrator in the loop, the VCO). The transfer function implies that while the (phase) frequency will be multiplied by N, the reference (φr) noise affects the output spectrum in a "controlled" way (Figure 10).

Example

Assume K = Kv * Kd = 28*10E6 sec^{-1}, and the crystal has a noise density of -165 dBC at an offset of 0.1 MHz from the carrier. For N=1000, the output noise at this offset due to crystal noise calculates to:- 105 dBC/Hz. However, because of the loop's ability to filter this noise, it can be much better than -105 dBC/Hz. The loop starts to attenuate this noise above 4400 Hz (K/N = 28*10E6/($2\pi \bullet 1000$)) from the carrier at 6dB/octave. At 100 kHz offset, the loop will attenuate this noise by more 26dB to below -131 dBC/Hz.

We can conclude from this analysis that a PLL is a narrow band multiplier, having the characteristics of a tracking filter. We shall see later that we can easily control the bandwidth of this filter, also known as the loop bandwidth.

Viewing the error transfer function $H_E(s)$, shows that it has "high-pass" characteristics. Therefore, we can conclude that the loop "resists" low frequency changes; it "tries to acquire" the characteristics of the reference source. If we try to inject a signal in order to modulate the VCO (say in FM applications), the loop will resist this disturbance, (see figure 10). Therefore, many FM systems, and especially those used in cellular applications, must use a very narrow band loop, so that the voice (300-3400 Hz) spectrum is significantly above the frequency where the loop has an effect (typical 20-30 Hz).

VCO noise can be modeled as additive; this noise will be rejected by the loop within the loop bandwidth.

Loop Filter Design

We saw before that when there is no loop filter, H(s)=1, the loop parameters were determined by K and N. This way, our control of the loop parameters is very limited and has already been set by K and N.

To gain complete control of loop parameters, (mainly bandwidth, noise characteristics and speed), the more common (2^{nd} order) and in fact the most popular loop structure uses (at least) another integrator, having a transfer function given by:

$$H(s) = \frac{1+sT2}{sT1} \qquad \text{(Equation 10)}$$

where: T1=R1C, T2=R2C (see Figure 13).

Now, the new loop transfer function is given by:

$$H1(s) = \frac{K(1+sT2)/T1}{s^2+K(1+sT2)/NT1}$$

Lets define: $\omega n=(K/NT1)^{.5}$ and $\xi=\omega nT2/2$, then:

$$H1(s) = N\bullet \frac{2s\omega n\xi+\omega n^2}{s^2+2\omega n\xi s+\omega n^2} \qquad \text{(Equation 11)}$$

This is the most common loop transfer function in PLL theory. The loop is of second order (has two integrators) and enables control of its dynamic characteristics, bandwidth and damping, via T1, T2, resistors and capacitor. This structure, with minor modifications, is used in most frequency synthesizer designs.

Natural Frequency and Loop Bandwidth

A normalized second order transfer function is shown in Figure 10.

ωn is referred to as the natural frequency, and ξ is the damping factor, both terms borrowed from control theory. For low values of ξ, the loop tends to oscillate. This is the reason for not using a pure integrator as a loop filter. Most designers use a damping factor between 0.7 and 2. The loop behavior is similar to many natural phenomena described by similar (second order) differential equations. There is a great body of literature covering this loop behavior, see the References and Further Reading section at the end of this document.

The solution of the denominator polynomial shows that:

$$S_{1,2} = -\xi\omega n +/- \omega n \sqrt{\xi^2 -1}$$

For $\xi > 1$, settling to lock state will be asymptotic. For $\xi < 1$, it will be asymptotic with oscillation, or "ringing", occurring at a frequency of $\omega n\bullet\sqrt{1-\xi^2}$.

The following is a review of the characteristics of this loop (see Figure 10).

The loop behaves like a low pass filter that is centered on the carrier instead of DC. (Actually, it is a bandpass tracking filter). This filter's integrated bandwidth (also referred to as noise bandwidth), is given by:

$$B_L = (\int |H1(j\omega)|^2 d\omega)^{.5} = \omega n (\xi+1/4\xi)/2 \qquad \text{(Equation 12)}$$

This is shown below, in Figure 10.

Figure 10. 2nd Order Loop Transfer Function. ξ = 0.7

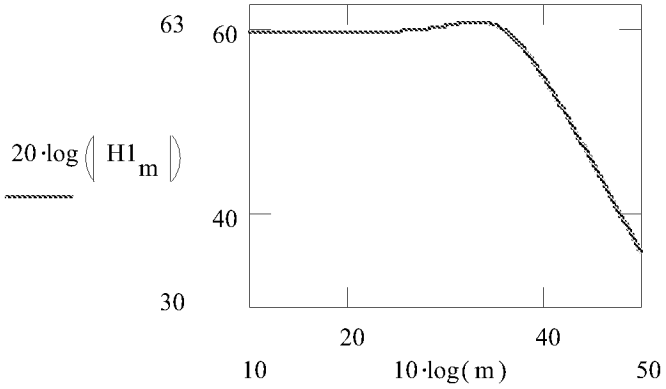
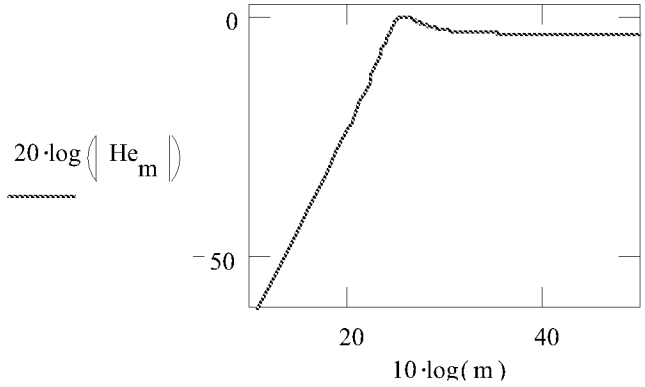


Figure 11. 2nd Order Error Transfer Function. ξ = 0.7



Minimum value for this function is for ξ = 0.5, there $B_L = \omega n/2$.

Figure 12. B_L Function of ξ ($j = 100\xi$)

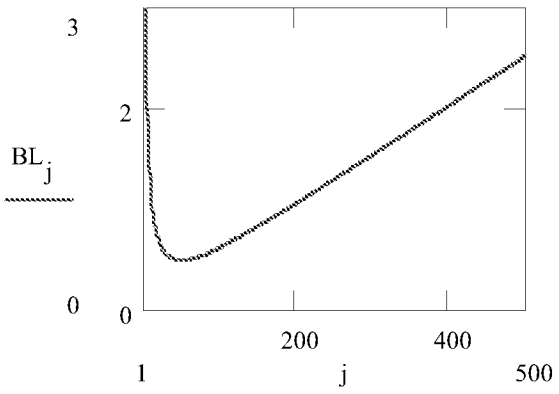


Figure 13. Active 2nd Order Loop Filters

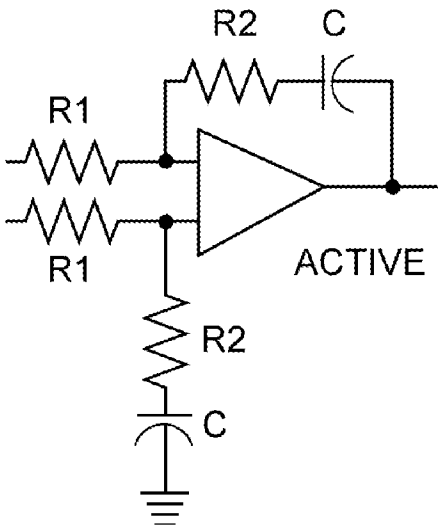
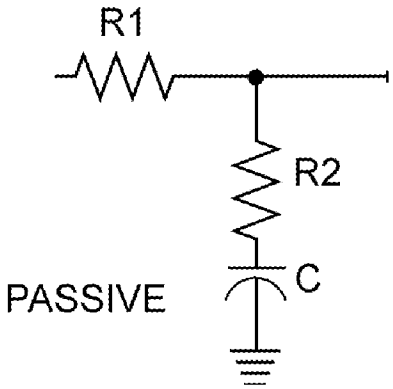


Figure 14. Passive 2nd Order Loop Filters



Though ωn is the natural frequency (the frequency at which the critically damped loop will oscillate when disturbed from equilibrium), it is also an indication of the loop bandwidth; a measure of its dynamic ability to track and follow the carrier as well as reject noise sources. Many designers refer to $\omega n/2\pi$ as the loop bandwidth. A more fundamental parameter, but not often used, is ωp, the frequency in which the open loop gain equals 1.

The loop bandwidth also indicates loop dynamics and the speed with which it will lock. The speed relationship (asymptotic behavior) depends on how far the new frequency we change to is, as well as other parameters (among them phase detector characteristics, ξ). Generally, loops with higher ωn will lock faster. Some of the speed up mechanisms actually increase ωn for the duration of the lock up (acquisition) time, to speed up the acquisition process.

Note that when ξ is very large, the 2nd order approximates 1st order characteristics as the effect of the capacitor is reduced (for very large R2, the op-amp transfer function approximates R2/R1). This is used in timing circuits to reduce "peaking" in the response.

Passive Loops and Charge Pump

In many applications, economics forbid the use of an active loop; also an active loop might not be necessary. For example, cellular synthesizers cover only 25 MHz, a 4% bandwidth. With a VCO that has a Kv = 12 MHz/V, there is no need to use any active interface between the phase detector and the VCO. Passive loops are then used and take the form of a lead-lag network such as the one shown in Figure 15.

The transfer function of this network [(R2+1/sC)/(R1+R2+1/sC)] is given by:

$$H(s) = \frac{1 + sT2}{1 + s(T1 + T2)} \qquad \text{(Equation 13)}$$

As a consequence, the difference in the loop equations is as follows:

$$\omega n^2 = \frac{K}{N(T1+T2)} \qquad \xi = \omega n(T2 + 1/K)/2 \qquad \text{(Equation 14)}$$

In high gain loops, (1/K<<T2), the equations of the active and passive loops converge.

Most common for wireless applications, the phase detector output is a current source (also referred to as charge pump) rather than voltage source. The design equations for the 2nd order loop (shown in Figure 15) are then given by:

$$\omega n = (K/NC1)^{0.5}$$
$$R = 2\xi(N/KC1)^{0.5} \qquad \text{(Equation 15)}$$

where Kv is in Hz/V
Kd is in A/rad
K = KvKd has dimensions 1/sec*Ohm. (Note: Ohm*Farad = Sec)

This network (R/C in parallel with an ideal current source) response is given by:

Vo/I = R+1/sC1

Therefore, the current to voltage transfer function Z(s) = Vo/I, is given by (1+sRC1)/sC1 (perfect integrator) and the closed loop denominator takes the form:

s^2+ KRs/N + K/NC1 (Equation 16)

Now ωn and ξ (shown above) are easy to derive.

Most PLL ASICs use a current source output for the following reasons:

1) It is the most convenient way to generate the analog output function of the phase detector with digital three-state devices (current sources, charge pump structure).

2) Assuming an ideal current source, the design has a real 2nd integrator (1/s) in the loop, compared with the voltage passive network.

3) Reference spurious signal attenuation by a 3rd order loop structure is easily attained by the addition of a single capacitor, (C2 in Figure 15).

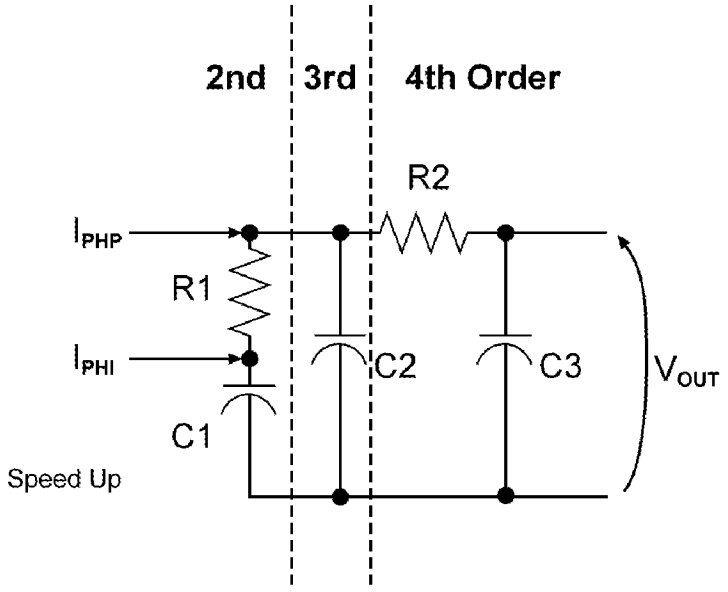
4) A single ended filter structure provides economy, compared to a differential circuit, for active loops.

As mentioned, most practical designs add a shunt capacitor (C2) between the current source output and ground (3rd order loop) to help attenuate spurious signals caused by reference spikes leaking out. The new network impedance transfer function is given by:

$$Z(s) = \frac{1+sRC1}{s^2\,RC1C2+s(C1+C2)} \quad \text{(Equation 17)}$$

For third order loops, (and higher), we must calculate the loop phase margin, to insure stability. (Note that 2nd order PLLs are inherently stable, if ξ > 0). 4th order loops add an extra R/C for additional spurious filtering.

Figure 15. Loop Filter for Current Source (Charge Pump) Phase Detector



Lock-up Time and Speed Up

Initial Lock-up

Because of the importance lock time has gained in the last few years, special techniques and circuits have been devised to improve this parameter. A PLL circuit, being a feedback loop, theoretically never achieves steady state, but always approaches that state asymptotically. Thus lock time is usually defined by approaching the final state to within some defined margin (i.e. +/- 1 kHz). In digital modulation applications, the receiving modem always has some frequency and phase tracking capability, so the frequency error tolerance is based on overall system performance requirements.

In second and third order loops, it can be shown that switching speed depends on ωn and ξ. When hopping by "dF" Hz and settling to "df" Hz away from the new frequency, the system will asymptotically converge to zero error such that $\delta f/\delta F$ is proportional to $e^{-t\omega n\xi}$, thus the switching time, Tsw, is given by:

$$Tsw = -\ln(\xi\delta)/\omega n\xi \qquad \text{(Equation 18)}$$

Example

Let:	df = 1 kHz
	dF = 20 MHz
	$\xi = 1$
Then:	$\delta = 1/20000$
	$Tsw = -\ln(1/20000)/\omega n \approx 10/\omega n$

The VCO will settle in $10/\omega n$ seconds to within 1KHz of the final frequency when hopping 20 MHz.

The speed with which the synthesizer can hop from one frequency to another is an increasingly important parameter. It is applicable as a diversity technique (narrow band signals suffer fading effects that are frequency dependant, hopping frequencies can attenuate this effect) as well as a networking protocol. Rather than operating in Frequency Division Multiplex mode in which each channel has a dedicated frequency, all channels are changed periodically in frequency to reduce the effects of multipath and external interference.

Speed Up Mechanisms

We saw that the loop parameters, ωn and ξ, determine speed. In most cases, the loop is designed for bandwidth and phase noise profiles. Sometimes, the outcome does not provide sufficient speed. To improve this parameter, simple and effective speed up mechanisms have been added to many ASICs (see the data sheets for Texas Instruments TRF2020, TRF2050 and TRF2052 circuits). Improvements of up to 5:1 are possible using simple circuitry.

One speed up mechanism performs "pre-tune" of the VCO to the desired frequency. This will expedite the time it takes the VCO to slew up (or down) and will bring it to lock proximity, where the loop can start settle and lock fast. Another technique is to increase ωn for a short time and speed up the "acquisition" time. This can be done by charging the largest capacitor in the loop filter directly, or even increasing the charge current in this short time, to expedite the charging process. One popular technique is to create a separate port that charges the capacitor in the transition. The "PHI" terminal of the TRF 2052 is a good example of this. Another method is implemented by an analog switch that bypasses the shunt resistor and allows charging of the capacitor directly. Terminal "SWM" in TRF 2020 is an example of this method. Speed up mechanisms can improve lock times by a factor of 1.5-5. Note that in the speed up mode, care must be taken to insure that the loop remains stable.

Loop Order and Type

Loop order is the number of poles in the closed loop equation denominator. Loop type is the number of poles at "0" in the open loop denominator. The 3rd order loop filter we demonstrated in Figure 8, has the open loop transfer function:

$K(1+sT2)/s^2(1+sT1)$ and is of type 2 and order 3. (Equation 19)

Loop Stability and Phase Margin

Control theory shows that for stability, the open loop phase at gain = 1 (0 dB) must be in excess of 180 degrees.

Intuition: since the feedback is negative, there is a feedback inversion of 180 degrees. The 2 poles of the 3rd order loop denominator shift the signal by another 180 degrees $\{(j\omega)^2=-\omega^2\}$, for a total of 360 degrees. Therefore an extra phase shift is necessary. Careful location of the extra pole and zero $[(1+sT2)/(1+sT1)]$, will insure stability.

Phase margin is defined as the open loop phase difference from 180 degrees at the frequency at which the open loop amplitude gain is unity. To ensure loop stability, the usual requirement is that the system have at least 40-45 degrees of phase margin. If C2<C1/10, this condition is easily met and is the reason this rule of thumb exists.

The two controlling time constants are now T1=R1C1 and T2= R1C1C2/(C1+C2). The open loop transfer function is:

$H_{OL}(s) = T1K(1+sT2)/[s^2 \bullet C2N(1+sT1)T2]$ (Equation 20)

The phase margin is given by:

$$\phi_M = 180 + tg^{-1}(\omega T2) - tg^{-1}(\omega T1) \quad \text{(Equation 21)}$$

Sometimes, the 3rd order structure does not provide sufficient reference spurious signal rejection. One option is to add an additional R/C circuit to further attenuate the reference spectral line. This will make the loop a 4th order type. Stability requires that the pole of this additional R/C structure be at least 10 times ωn; thus we require $1/(R2*C3)>10\omega n$ (see Figure 15). Following this rule insures an additional phase shift of no more than 4-5 degrees. A simulation program is useful to calculate the total open loop transfer function and its phase shift before the design is implemented. This will insure that at the frequency where gain is 1 the phase margin is still at least 40-45 degrees, including manufacturing tolerances. Equation 22, below, is the transfer equation.

$$H4(s) = \frac{T1K(1+sT2)}{T2s^2\, N(1+sT1)\,(1+sR2C3)} \qquad \text{(Equation 22)}$$

Figure 16. Open Loop Phase of a 3rd Order Loop

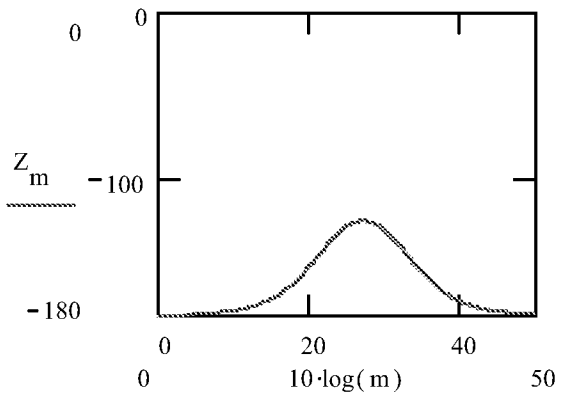
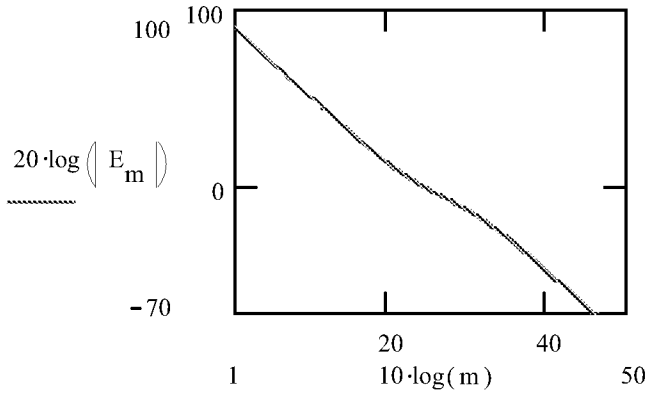


Figure 17. Open Loop Gain of a 3rd Order Loop



Active and Passive Loops Summary

The following is a short summary of various loop structures and design procedures. When possible, passive loops are used for simplicity and economy; otherwise, active loops using op-amps must be employed. In most cellular and PCS applications, the overall bandwidth is narrow (3-5%) and the output voltage from the PLL chip is sufficient to cover the band (including manufacturing tolerances). These use passive 3rd and 4th order loops. If wide-band synthesizers are necessary, (Satcom applications require 10-15 V for the VCO control) a larger (than PLL chip supply) control voltage must be generated and op-amp integrators are used. When using op-amps, differential connection is implemented. Low noise op-amps will not add significant noise to the PLL circuit.

Below is a summary of the design equations.

For 3rd order passive PLL design (most wireless applications):
Given Kv in rad/secV and Kϕ in A/rad
$\omega n = (KvK\phi/NC1)^{0.5}$
$\xi = .5 \bullet R1(KvK\phi C1/N)^{.5}$

and C2<C1/10

Tsw, switching time for convergence to df for a dF excursion is given by:
$Tsw = -\ln(\xi df/dF)/\xi\omega n$

If another R/C is required to further attenuate reference spurious signals, make sure that:
$R2C3 < 1/10\omega n$

Phase margin for a 3rd order loop:
$\phi_M(\omega) = tg^{-1}(\omega T2) - tg^{-1}(\omega T1) + 180$

For 2nd order active loop:
$\omega n = (KvKd/NT1)^{.5}$
$\xi = \omega n \bullet T2/2$
Here, Kv is in rad/secV and Kd in V/rad.

Modulation

Amplitude Modulation (AM) and Phase Modulation (PM) are usually performed outside of the phase locked loop. AM is performed by multiplying the carrier, $Sin(\omega_0 t)(1+m\sin\omega_m t)$, using mixers or other analog multipliers. PM is performed by complex multiplying, using quadrature modulators. This yields:

$Sin(\omega_0 t)R(t) + Cos(\omega_0 t)R\text{-}(t)$

R(t) and R-(t) are the quadrature components of the baseband information.

Generally, R-(t) will be the Hilbert transform of R(t). A variety of monolithic wide band quadrature modulators are available from various manufacturers. (The TRF 3040, soon to be released from TI, is a fractional-N monolithic PLL ASIC with an on-board quadrature modulator). R(t) and R-(t) are usually generated from a ROM or other digital memory that calculates the exact values and generates the analog signal for modulation via a Digital to Analog Converter, DAC.

Frequency Modulation (FM) can be performed by modulating the VCO directly. If a signal, V_{FM}, is injected after the loop filter on the input control line to the VCO, its transfer function is:

$$\varphi_0/V_{FM} = Kv/s/(1+KH(s)/sN) = NKv/(sN+KH(s)) = H_{FM}(s) \quad \text{(Equation 23)}$$

For a second order loop, calculating (frequency) $df_0 = sd\varphi_0/2\pi$:

$$sH_{FM}(s)/2\pi = s^2 G_L/(s^2 + 2\omega n\xi s + \omega n^2) \quad \text{(Equation 24)}$$

where G_L is a constant.

Within the loop bandwidth, the modulating signal will be attenuated (s^2 in the denominator). Two options can be utilized to compensate for the loop attenuation, depending on the application:

1) The loop is made very narrow, as in cellular FM. Beyond the loop bandwidth the transfer function becomes GL, (for $s>>\omega n$, $s^2/(s^2+2\xi\omega n+\omega n^2) \approx 1$) a constant, and will not affect the modulator. In FM cellular, the voice spectrum is >300 Hz, and loop bandwidth in the order of 30-50 Hz.

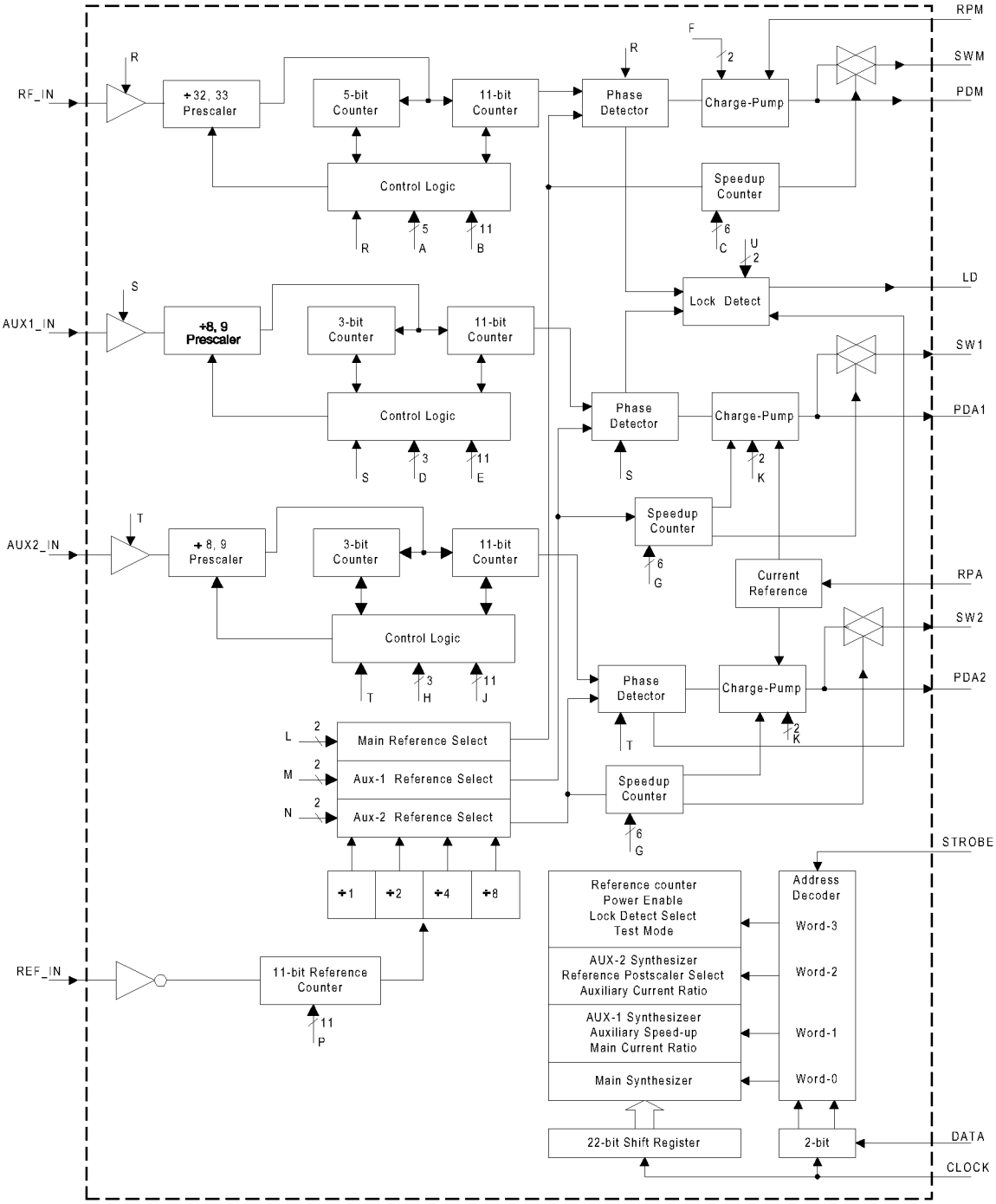
5) If the loop must be kept somewhat wide (more than 15 - 20% of the modulating frequency), then the effect of the loop must be compensated. This can be done by passing the modulating signal through a network that compensates (pre-distorts) for the transfer function. Usually, this takes the form of an integrator. More complex schemes can be applied to improve low frequency response by modulating (injecting signals) at more than one point (VCO input and PFD output).

Integer-N PLL

Concept

We can now describe in detail the "nuts and bolts" of classical, integer-N, PLL circuits. Let us review detailed functionality by describing the Texas Instruments TRF2020 PLL ASIC which is equipped with all necessary functions (see Figure 18). Let's review the operation of the main RF synthesizer, shown in the upper part of the schematics in Figure 18, below.

Figure 18. Integer-N PLL Circuit Detail



Basic Operation

The RF section of the PLL circuit consists of the following basic blocks:

- A control interface that allows the setting of parameters (such as counters, current source values, switch mode, sleep, others) and controlling the synthesizers using an external computer/controller
- Crystal oscillator input for reference generation
- Dual modulus device (32/33)
- Reference, Fx, and main, M, A, counters. [Total divisor N is A•(P+1)+(M-A)•P. A and M are controlled by the interface.]
- Phase Frequency Detector
- Lock indicator - monitors when the loop is locked (or out of lock)
- Speed up circuit
- Power down mode (usually with a few μA current draw in this mode)
- Separate power supply pins for phase detectors allow running the device at low supply with higher output voltage from the phase detectors to control VCO across a wider range.

Functional Description

The synthesizer is set by the three wire standard interface for a specific reference frequency (the division needed from the crystal frequency to generate the reference Fr) and the division ratio of the VCO such that Fvco/N = Fv = Fr. A detailed interface protocol is available with the data sheet. The crystal reference signal is connected to the Ref input and divided by R (the P counter in the drawing). The reference (Fr = Fx/R) is compared to the VCO signal after division (Fvco/N) in the phase detector and the error signal then connects via a loop network to the VCO.

The RF signal from the VCO is first amplified (to internal logic levels) and buffered before being connected to the dual modulus divider. The input amplifier provides sensitivity (-15 dBm) and buffering from the divider (otherwise divider generated spurious signals will show at the output).

The total division (N) is determined by the number of times the dual modulus divides by P or P+1 (it is 32/33 in this case). The phase detector is a current source (charge pump) output and was designed for passive loop applications in wireless designs. Though the dual modulus device operates dynamically, dividing by 32 (M-A times) and by 33 (A times), the signals arriving at the phase detector inputs are periodic and therefore “orderly” (compared with fractional-N architectures that are not). In lock conditions, the frequency and phase (rising or falling edge) of Fr and Fvco/N will coincide (see Figure 8).

Phase Interpretation

Since there are "N" VCO clock ticks in every Fr cycle, a VCO tick counts as 360/N degrees completing a cycle (2π of Fr) in N ticks. For example, when generating 900 MHz from a 30 kHz reference (N = 30000), every VCO cycle is only 360/30000 = .012 degrees of Fr.

Divider control: for the generation of total division of 30,000, M = 937 and A = 16. This way, 16•33+(937-16)•32 = 30000.

The general formula can be derived easily:
30000/32 = 937.5.
So M = 937 and A = .5x32 = 16.

This way, a controller can easily calculate any number desired.

The supply voltage, VDD, operates all functions and can be as low as 2.7V. The phase detector supply has a separate pin that can operate up to 5.5V and allows wider VCO control range. The output of the Phase Frequency Detector controls the current sources and, in lock, will generate a DC signal. The most common loop network consists of a shunt capacitor and a R/C network, a 3rd order structure. Assuming an ideal current source, the R/C transfer function was given already. For an ideal current source (infinite output impedance), the network will represent a perfect integrator. In reality, the current source has finite impedance, Ro, and the accurate 2nd order transfer function can be modified from:
(1+sT1)/sT1
to
Ro(1+sT1)/(1+sT1+sCRo), known as a "bleeding" integrator.

Usually, an extra capacitor is added to filter out Fr pulses that show in the phase detector output pin. The time constants which determine the pole and zero frequencies of the transfer functions are defined as T2 = R1C1C2/(C1+C2) and T1 = R1C1. For C2<C1/10, T2 $\approx$ R1C2. This is the most common configuration for loop filters in wireless applications. T1 and T2 are set independently and C2 on the output port (the phase detector output) helps attenuate spurious signals. The popularity of this configuration is due to the fact that compared to an active loop, no operational amplifier is necessary and the loop is single ended, thus providing simplicity and economy.

Phase detector output (PDM in this device) current can be controlled by the function RPM. RPM can be one of four levels, up to +/- 2mA (K_ϕ = .002/2π A/rad). The SWM function (in the PFD output) allows speed up of lock time by pumping more current during the transition (charging the capacitors faster) with a capability of up to 2mA (2mA will charge a .01μF capacitor to 2V in 10μsec). When activated, the phase detector output, SWM, connects directly to the capacitor, bypassing the external loop resistor R1 (see Figure 18) and often pumping more than the PFD nominal current. After the switching transient, the SWM port goes to a high-impedance (Z) state, operating like an analog switch for the duration of the transient. The programmable speed up counter, field G, controls how long the speed up lasts (in number of reference clock cycles), so its total time is: 2*G / Fr where 0<G<64. For G = 40, with Fr = 30 kHz, speed up lasts 80/30,000 = .26 ms. In some PLL chips the speed up time in controlled by the width of the LE programming pulse.

The two Auxiliary PLL functions, AUX1 and AUX2, are very similar to the functionality of the Main PLL, except that both use a dual modulus prescaler of 8/9, compared to 32/33 of the main loop.

Advantages and Limitations

A circuit like the TFR2020 is a typical integer-N synthesizer chip. Other PLL chips in the market offer single or dual similar functions. These provide functionality, low power, space saving and economy. The device will synthesize one RF and one or two IF frequencies in a wireless radio applications for IF processing or clocking. Such devices have become the basis of wireless synthesizer technology, operating at low voltage and low current. Switching speed can be enhanced to the sub-millisecond range. One major deficiency (when critical) is the high division ratio (when generating high frequencies with small step size), thus causing significant degradation in phase noise performance. Integer-N PLL chips in the market have phase detector (PFD) noise floors of -165 to -145 dBC/Hz with 10-100 kHz Fr reference. (Noise levels usually increase with an increase in Fr). For most analog systems (FM), phase noise of such levels is sufficient. However digital technologies are more sensitive to phase noise and require more stringent control of spectral noise. Most QPSK modulations require phase jitter of <2° rms.

Some manufacturers specify PFD performance as a function of Fr speed. A general rule of thumb is that phase detector noise will increase 10 dB per decade-increase in Fr. Phase noise increases with Fr speed due to the following relationship: the time in which the phase detector (charge pump) is active (during lock) is fixed and due solely to the device architecture and speed. As the reference frequency increases, the phase detectors are active more often (their duty cycle increases) over a given time period. This adds more noise to the circuit. Other parameters have effect too like circuit symmetry, switching speed, and current output.

Fractional-N PLL

Concept

Fractional-N architecture allows frequency resolution that is a fractional portion of the reference frequency, Fr. Therefore Fr can be higher than the step size and overall division (by N) can be reduced.

The main motive for using fractional-N architecture is to improve phase noise; however, increasing Fr makes it possible to improve switching speed as well by increasing loop bandwidth.

The output frequency in fractional-N designs is given by Fvco = Fr (N+K/F), where F is the fractional resolution of the device with respect to the reference frequency.

Example: If we require 30 kHz channel spacing and have a fractional resolution of 16, Fr can be 480 kHz and N is reduced by a factor of 16.

This reduction of N implies a theoretical reduction of 20log(16) = 24 dB in phase noise performance. For a 900 MHz design, the total division ratio, N, will be ~1800 rather than 30,000 for integer-N architecture. The concept of fractional-N is achieved by generating a divider that is a fractional number rather than an integer. This is done by changing the divider in the loop dynamically, between the values N and N+1 in such a way that the “average” division becomes a fraction N+K/F. If out of F cycles, we divide by N+1 K times and by N, F-K times, then the average division is N+K/F. The principle of fractionality is therefore a result of averaging, as there is no device that can divide by a fraction.

Functional Description

Fractional-N architecture is very similar to integer-N, with the addition of an accumulator. The accumulator is a simple state machine that changes the main divider value (between N and N+1) during a locked condition. The accumulator varies the divide number between N and N+1 dynamically in such a way as to provide an averaged divide ratio that is a fractional number between N and N+1. This function enables the generation of an average division that is a fractional number.

For example: If N = 2000 and Fr = .48 MHz, the output frequency is as follows

Fvco = 2000•(.48) = 960 MHz.

In order to achieve 30 kHz resolution (generate 960.03 MHz for example), the accumulator must dynamically change N from 2000 to 2001 one out of every 16 reference cycles. Thus the division will be set to 2000 for 15 cycles of Fr and set to 2001 for one cycle of Fr. Therefore, the average division will be 2000+1/16.

(15•2000+1•2001)/16 = 2000+1/16. Here F = 16 and K = 1.

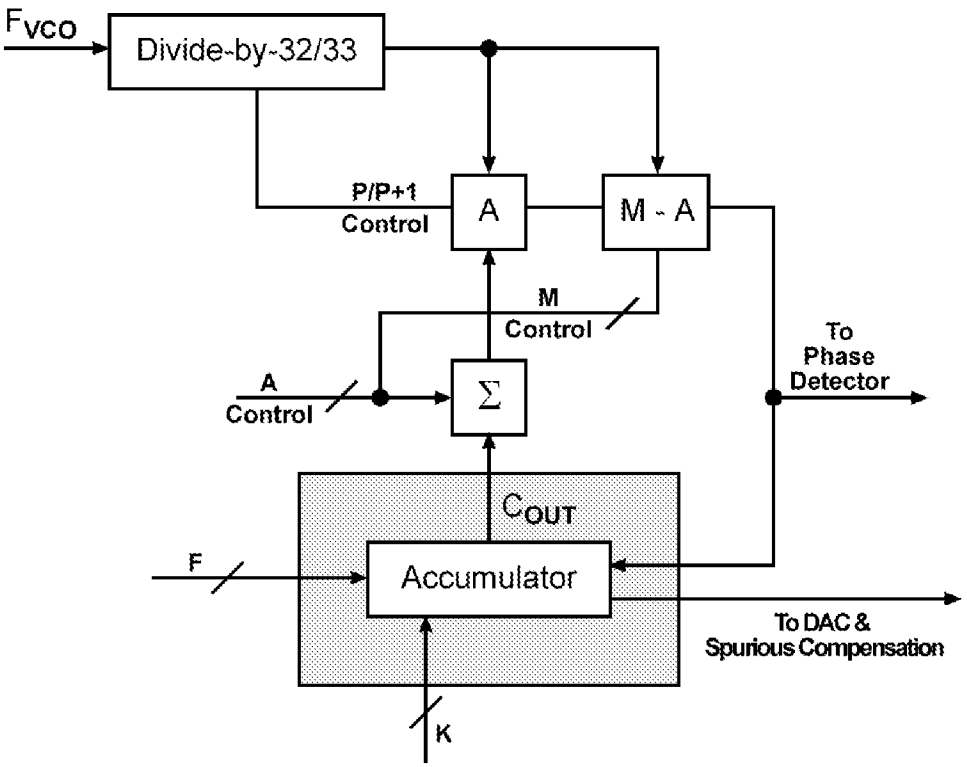
So far, we have created a fractional divider. However, rather than generating a smooth N+K/F ratio, it was done in an abrupt manner. This will cause spurious signals in the output. A spurious compensation circuit is added to reduce these spurious signals to a practical minimum.

Divider Dynamics

In integer-N PLL, the division ratio N is fixed. Every reference cycle period, 1/Fr sec, the VCO frequency is divided by N. In fractional-N, an average division of N+K/F is achieved by dynamically changing the division in such a way that in F reference cycles, K times the divider is N+1 rather than N. Thus, over F reference cycles, the total division is N*=K(N+1)+(K-F)N, and the average N*/F=N+K/F. Because there is no device that can divide by a fraction, the fractional divider value is achieved by averaging.

The elements of fractional-N (dual modulus, counters M, A) already exist in integer-N, but they need to be implemented and expanded. Remember that in integer-N, the total division is reached by commanding the dual modulus to divide A times by P+1 and M-A times by P so that N=A(P+1)+(M-A)P. Now, if from time to time, K times in F cycles, the value of A is incremented by 1, N also increments by 1 [note that (A+1)(P+1)+P(M-A-1)=N+1]. All we need to do is to add the mechanism to dynamically change the value of the A counter. The fractional accumulator performs this function (see Figure 19).

Figure 19. Fractional-N Accumulator (will change N to M)



Fractional Accumulator

Every fractional-N PLL contains a block of circuitry that is referred to as a fractional accumulator. This accumulator enables the IC to dynamically change the N divisor value *during* the locked state of the PLL (see Figure 19). The timing of the accumulator is clocked by the VCO signal (after division by N). Each time the accumulator overflows, the carry out goes from LOW to HIGH and the counter N is commanded to increment to N+1. In a system sense, K is the programmable value that is equal to the number of times the device will divide by N+1 in a full fractional divide cycle and F is the value that determines the number of reference cycles that are in each full fractional divide cycle. In actuality, F represents the size of the counter in the accumulator (i.e. F = 16 means the counter is a 4-bit counter that can count from 0000 to 1111) and K is the value that is added to this counter at the end of each reference cycle.

For example: with F = 16, and K = 3, the value of the accumulator over a full fractional divide sequence will be (see Figure 20):

0, 3, 6, 9, 12, 15, (↑2), 5, 8, 11, 14, (↑1), 4, 7, 10, 13, (↑0)

A total of 3 carry-outs (↑) occur over 16 reference cycles. Because each carry out forces the N divider to divide by N+1 for one reference cycle, the average divide ratio becomes N + 3/16.

In general, when writing to the accumulator the value K, the average division is as follows:

$$(N(F-K)+(N+1)K)/F = N+K/F=N^* \quad \text{(Equation 25)}$$

When the value at the accumulator output is not 0, (say 3 or 6), it indicates that there is a phase error between the reference (Fr) and the feedback, Fvco/N*. This phase error increases proportionally with the accumulator value (i.e. 3, 6, 9, 12, and 15) until an overflow occurs and the main divider is incremented by 1.

Note two important principles: first, we wish to increment the VCO carrier by K•2π each F cycles of Fr. The accumulator performs this function. Second, an accumulator is a digital integrator. Over F cycles, it will accumulate the value K•F, and will therefore generate precisely K carry-outs (hence a duty cycle of K/F).

The result of incrementing (by one) the value of the N divider for one reference cycle is that a full cycle of the VCO (2π), is "swallowed" and the phase error between Fr and Fvco/N is decreased by 2π. The accumulator insures that this phase error is never above 2π. After the "swallowing", the phase error continues to accumulate. The actual instantaneous phase error between Fr and Fvco/N* can be calculated at the end of any reference cycle using the following equation:

Phase Error (radians) = (2π/F) • accumulator value

The end of a full fractional divide cycle occurs when the carry over value is equal to zero. Therefore the period of a fractional cycle is every (Fr/F) Hz.

This means that the periodicity of the phase detector output is equivalent to that of integer-N designs (with equal channel spacing), though the reference spur is now at Fr Hz away from the carrier.

Of course the abrupt change in phase associated with N being incremented by one on a periodic basis will also cause a spurious signal. This spur is called the fractional spur and can be located as close as (Fr/F) Hz away from the carrier. Although the PLL has generated the correct "average" phase slope to lock to the fractional channel, it has done so via abrupt changes in the phase slope that must be quantized in integer multiples of 2π. This spur will be of greater magnitude than a typical reference spur and also reside on the adjacent channels in worst case channel settings [1/F and (F-1)/F fractional channels]. In general applications, the fractional spur must be suppressed in some manner other than by the loop filter for this technology to be useful.

Fractional Spurious Signals and Compensation

The spurious signals generated by the accumulator can be calculated exactly by convolution of the PLL loop filter response with the Fourier series coefficients of the abrupt waveform described above. With no loop filter (i.e. infinite bandwidth), spurious signals can be approximated as $20\log(2\pi/2\sqrt{2})=7$ dBC. In this case, the fractional spur will be 7 dB higher than the carrier signal. This is much larger than the typical reference spur generated by an integer-N device.

If the fractional resolution (Fr/F) is large relative to the loop bandwidth, the spurs can be easily filtered out by the loop with the addition of low pass or notch filters. For the general case of wireless communications (typically 10 kHz to 200 kHz channel spacing) traditional loop filtering will not be sufficient and the fractional architecture we described loses appeal as a synthesis method. A very narrow loop filter would result in excess phase noise and very poor lock times, offsetting any other merits the fractional architecture has. Fortunately, the fractional spurs generated by the accumulator can be reduced by as much as 40 dB (prior to loop filtering) through compensation circuitry.

The following discussion shows how the designer can compensate for these spurious signals (second order fractional) without lowering loop bandwidth.

So far we have used only the accumulator carry out to adjust for the phase error of the signal. This limits our resolution to 2π and prevents us from further attenuating the fractional spurs. If we review the accumulator content (not just the carry out), we observe that it represents the exact phase error at the end of every reference cycle. Therefore, the contents of the accumulator can be used to correct the instantaneous phase error; theoretically, we could generate a spurious free signal.

Let's consider the case for F = 8 and K = 1. Now, after the first Fvco/N cycle, the phase error (between the reference and VCO signals) is $2\pi/8$ radians, after the second cycle it will be $2*2\pi/8$ radians, and after i reference cycles the phase error will be $i \bullet 2\pi/8$ radians. It is no coincidence that i is the exact value that the accumulator holds at the end of each reference divide cycle. The same process holds true for any value of K.

To summarize, the accumulator with size F will generate K carry out transitions in F cycles. The accumulator content will represent the exact phase error necessary to be compensated at the end of each phase detector cycle:

$$\text{Phase error} = i \bullet 2\pi/F \qquad \text{(Equation 26)}$$

Where: i is the value in the accumulator
F is the fractional resolution of the device

Thus the information needed in order to compensate for the phase error is in the accumulator contents and the quality of the compensation depends only on the accuracy of the analog mechanism used to implement the correction.

For a binary accumulator, the carry out signifies 360 degrees, MSB bit represents 180 degrees, second MSB represents 90 degrees and so on. Generally, bit B from MSB represents phase $180x2^{-B}$ degrees. This is similar to the phase weight in DDS accumulators (for those unfamiliar with DDS synthesis operation see Reference 1, listed on page 54).

Table 2. Bit Weighting in a Binary Accumulator

Bit	Phase weight (degrees)
MSB	180
MSB-1	90
MSB-B	$180x2^{-B}$

For a general F size accumulator, (not necessarily binary), each increment value in the accumulator has a weight of 360/F degrees of phase error. For example, if F = 5, each bit has a phase weight of 360/5 = 72 degrees. These phase values (360*i/F) can be used to shift the VCO phase by pumping the corrective current value to the phase detector output.

Because the charge pumps “push” and “pull” current in order to change the phase of the VCO, the accumulator contents must be converted to current. The current must be scaled appropriately to correct the phase error at the end of each reference divide cycle. This current must then be added to the output of the phase detector (see Figure 22 and Figure 23). If the accuracy of this current correction is perfect, the phase correction interpolation is equal to the exact phase increments needed and all spurious signals will be cancelled (see Figure 20). Any error in the exact current used to compensate for the phase error will be periodic and will generate spurious signals with a level proportional the amount of error. Since this is an open loop analog circuit, careful design must be exercised to ensure amplitude and timing accuracy as well as temperature stability.

Figure 20. Fractional Spurious: Accumulator Only (2π Jumps Broken Line) and Analog Compensation (Straight Broken Line)

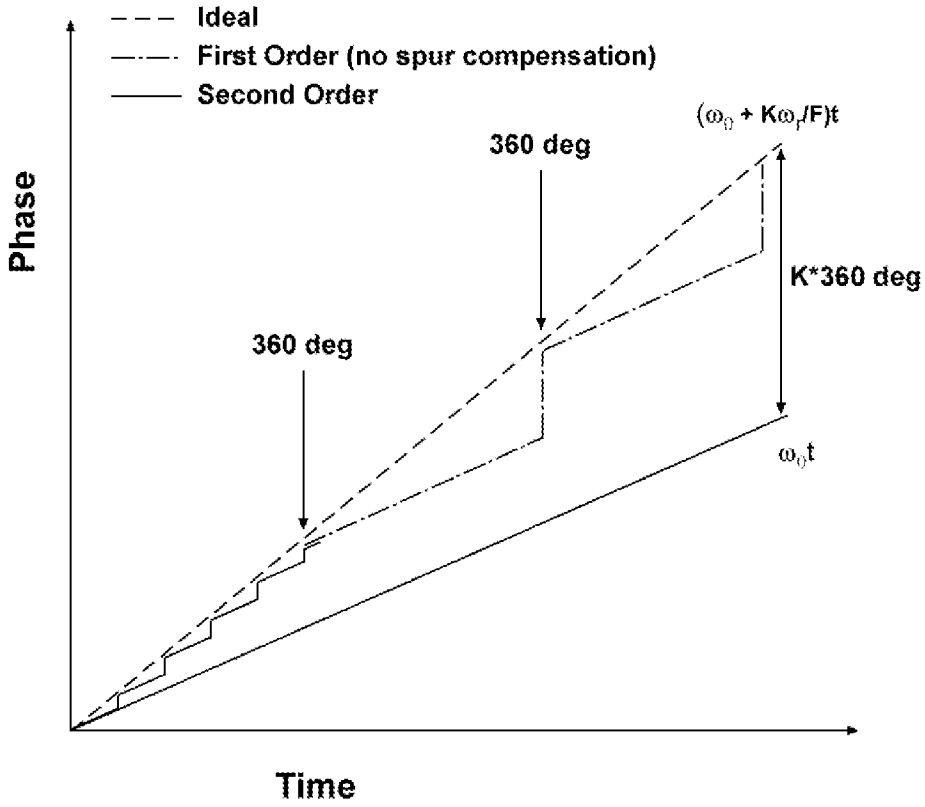
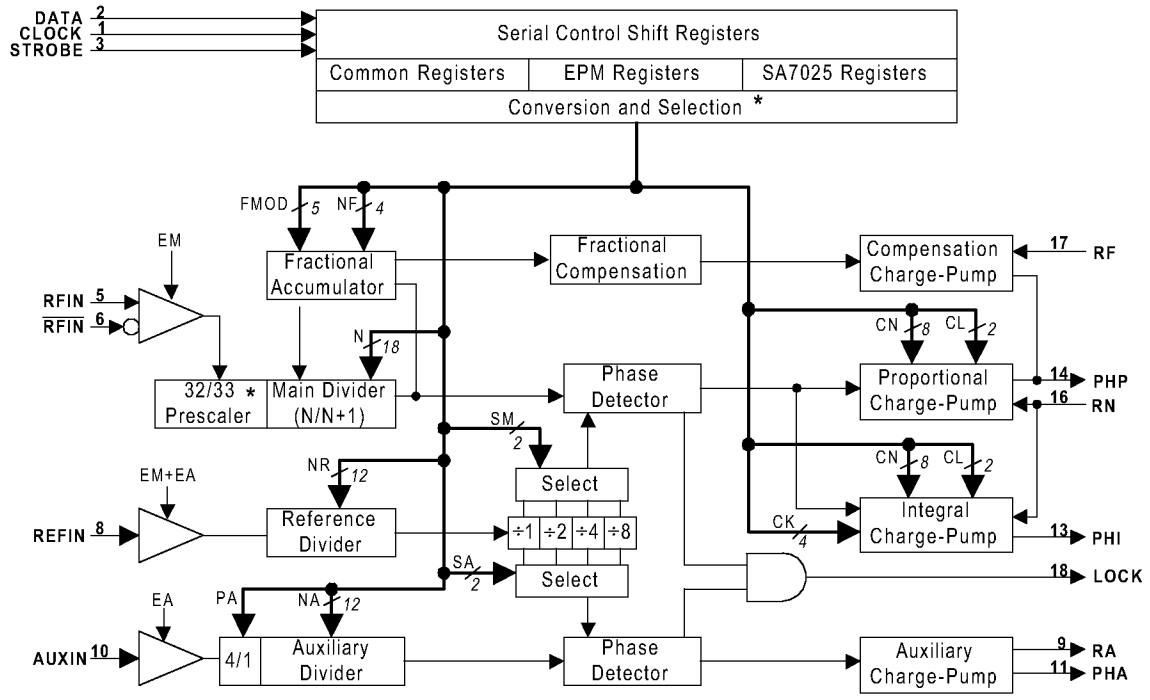


Figure 21. Fractional-N PLL - TI Model TRF2050



There are a variety of ways to implement such a compensation circuit. In a typical implementation, the accumulator (NF = 4 bits) can be any arbitrary value between 1 and 16. Its carry out connects to the main divider via an adder to allow a change in the total division ratio every time the phase error reaches 2π. The accumulator contents bits are connected via a digital to analog converter (DAC), in the Fractional Compensation block, to the output of the phase detector. If perfectly compensated, the DAC current will perfectly interpolate the phase increments at the 1/Fr time intervals. In reality, the cancellation is limited to overall accuracy, stability, aging, and temperature variation of the analog parts controlling the mechanism. The best case reduction in spurious signals is typically never better than -40 dBC. The loop filter (low pass) will further attenuate and help bring this level down to the -70 dBC range.

To improve user control of ASIC tolerances, the TRF2050 provides compensation correction control via software field CN (8-bit resolution), which helps optimize the compensation current value without the use of adjustable devices (potentiometers). This provides manufacturing convenience and economy.

Let us follow a specific detailed example for clarification.

Suppose N = 2000, F = 16 (4 bit binary accumulator) and K = 5, using Fr = 480 kHz. F = 16 indicates that the synthesizer step size is Fr /16 = 30 kHz. K = 5 indicates a desired output frequency given by: 0.48(2000+5/16) = 960.15 MHz.

Starting with an empty accumulator, after the first Fr cycle (1/.48 ≈ 2.08 μsec), the uncorrected VCO output develops a phase error given by 2π•5/16 radians. The content of the accumulator is exactly five. The following chart shows the phase error sequence (in multiples of 2π/16):

0, 5, 10, 15,↑ 4, 9, 14, ↑3, 8, 13, ↑2, 7, 12, ↑1, 6, 11, ↑0 ...

The DAC will compensate by extrapolating the abrupt phase change, and eliminate most spurious signals by feeding forward this error to the phase detector. Spurious signal compensation must be very accurate. (Phase accuracy has to be in the 1 degree range, translated at 900 MHz it is equivalent time accuracy of 3-4 psec and DAC current accuracy of 4-5 μA).

A detailed timing drawing is shown in Figure 22 (for K = 3). Complete functionality is shown in Figure 21. Note that when K and F have a common divisor higher than 1, (say Greatest Common Divisor GCD(K,F) = g) periodicity will be gFr/F, and spurious signals will show only there. Example: for F = 16 and K = 4, the spurious signals will show only in Fr/4 and its harmonics. If Fr = 240 kHz, F = 8 (step is 30 kHz) and K = 2, spurious signals will show at 60 kHz and120 kHz but not at 30 kHz since GCD(8,2) = 2.

Figure 22. Fractional-N Phase Detector Ripple for 3/8 Channel

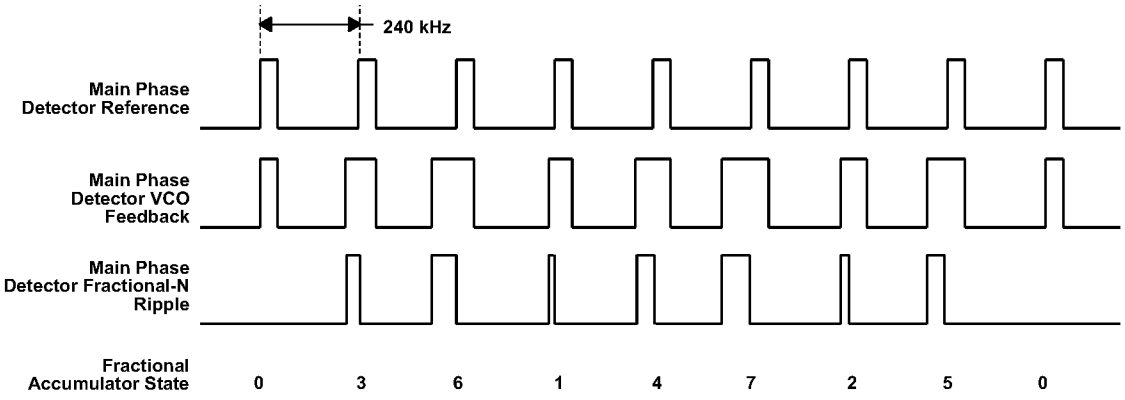
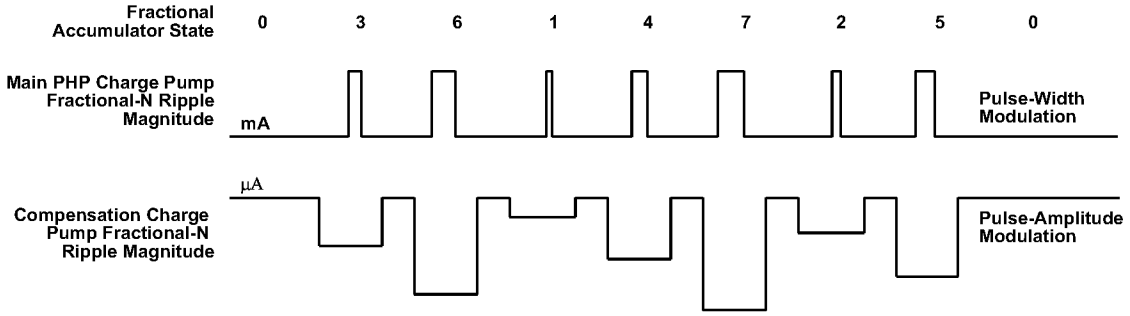


Figure 23. Main PHP and Compensation Charge Pump Fractional-N Waveforms for 3/8 Channel



Advantages and Limitation

Fractional-N architecture represents a rather simple but significant evolutionary progress of PLL architectures and does not have any major disadvantages. The additional complexity is modest, having minimal impact on power and cost, and the effect of the compensation circuit on phase detector noise density is minimal.

New fractional-N chips in the market are the products of the most advanced mixed signal IC technology. The limitations in spurious signal cancellation are mainly in the accuracy of the analog compensation circuit and its stability with time, process, and temperature changes. However, the technology already delivers spurious suppression levels of 30-40 dB prior to loop filtering. The mechanism is open loop and does not contain inherent correction. However, Texas Instruments (and others) provide programmable compensation, CN, to allow optimal control of the spurious signal levels in any given application and loop gain. Since the whole circuit is on a single die, temperature changes affect all circuits simultaneously and temperature stability is improved.

General advantages of fractional-N are the lowering of the division ratio, lowering phase noise, and improving dynamics by increasing the reference frequency. There is the potential to improve switching speed due to faster phase detector frequencies and possibly wider loop bandwidths.

When using fractional-N, while increasing Fr, we also increase the 1/F noise generated by the PFD. Therefore, we do not gain the theoretical 20log(F) in noise reduction. Typical gains are about half of that, 10log(F), which is very significant. Fractional compensation, being an analog open loop process, has achieved remarkable performance and should not be considered a limitation (as it used to be in the past). The ability to use higher reference frequencies opens the technology to applications not possible before, and allows very high frequency resolution that previously required multi-loop design.

Comparison

Fractional-N PLL represents significant progress in PLL technology. Compared to integer-N architectures, fractional-N requires a slight increase in complexity, (10-25 % in silicon area) but offers significant potential improvement in phase noise performance via reduction in division ratio. The use of higher reference frequency (Fr) offers an opportunity to widen loop bandwidth and achieve significant improvement in switching speed.

In addition, fractional-N offers high resolution in applications that would not be possible with integer-N. When step size needs be very low, integer-N collapses due to very high division ratios. This requires the use of multi-loop designs that are typically complex and expensive. Fractional-N design, due to the compensation accuracy, allows economical single loop solutions. For a 900 MHz design and 2 kHz frequency resolution, integer-N requires a division ratio of 450,000 that will result in ~116 dB in noise corruption. Such a design will have to use a very narrow loop bandwidth (< 20 Hz) to reject spurious signals and will become very sensitive to mechanical vibration. With fractional-N, with Fr = 32 kHz, and F = 16, the frequency resolution can be achieved using cellular design parameters (loop bandwidth of 200 Hz and more).

The compensation technology has matured to the point that fractional spurs (at Fr/F and its harmonics) are significantly lower than the reference spur. In fractional-N, Fr is no longer on the adjacent channel frequencies and therefore easy to filter.

The integer and fractional technologies complement one another. The statements above do not imply that fractional-N is going to replace integer-N. However, fractional-N advantages are significant, and will affect PLL evolution and market share.

Speed up is available in both techniques; however, fractional-N will usually result in faster lock times (for equal loop bandwidth) because of higher Fr. Fractional-N can be much faster as it allows the possibility of a wider loop bandwidth for similar spur suppression requirements.

All PLL devices discussed are comparable in power consumption, package size and cost. Fractional-N has a more complex phase detector and might lose some noise performance; however, this should not be significant. As a rule of thumb, fractionality (F) improves noise performance by 10log(F). Therefore from the practical standpoint, fractionality will improve phase noise by one half (in dB) of the theoretical potential. This might improve as PFD technology and device speeds improve.

We dare to predict that fractional-N is the future direction of PLL technology.

Table 3. Short Summary of TRF2050 Parameters

Parameter	Main	Auxiliary
Frequency (MHz)	1200	250
Supply	2.9 - 5.1 VDC	2.9 - 5.1 VDC
PD supply	Same	Same
Current (total)	7.5 mA	
Std. By Current (total)	<200uA	
Speed Up	Yes	No
PD Current (PHP)	2.5 mA	
PD Current (PHI)	6.0 mA	
Sensitivity (dBm)	-20	200 mV ptp
PD Current		0.25 - 0.5 mA
Ref input (MHz)	40	
Fractionality	0 to 16, programmable	No

Phase Noise

Phase noise is probably the major technical concern of frequency synthesis design. An overall radio specification will impose significant requirements on size, power dissipation, voltage requirements, cost and spectral purity. Of all the requirements, phase noise is the most challenging to the synthesizer designer. This chapter describes the definition of various interpretations of phase noise, derives the equations necessary to calculate various noise sources and offers techniques to reduce phase noise and its effect on communication channel performance.

Definitions and Conversions

Ideal deterministic waveforms, expressed as $s(t)=A \bullet \sin(\omega_0 t)$, do not exist in the real world. All real signals are narrow band noise. Thus, phase noise is our method of expressing the signal's spectrum. An ideal signal has a spectral representation of $S(\omega)=A\delta(\omega-\omega_0)$; its total energy is concentrated in a singular frequency. Real signals have a spectral distribution, and their energy is spread. The better the signal's quality, the more energy is concentrated close to the carrier.

Typically, we describe signals as $S(t)=A(t)\sin(\phi(t))$. Amplitude noise, A(t), can usually be contained to relatively low levels, with a noise density lower than -150 dBC/Hz. The more critical issue is phase noise, $\phi(t)$. The terminology (-dBC/Hz) suggests that signal perturbations caused by noise have a statistical spectral density measured in relative power to the signal's total power. –150 dBC/Hz means that in 1 Hz bandwidth at specified offset (Hz) from the carrier, the (single sideband) noise power is 10^{-15} of the total signal power. Low frequency offset noise (from DC to 100 Hz offset from the carrier in wireless) is generally attributed to the crystal oscillator slow drift caused by aging, temperature and flicker factors. This is the "long term" noise, mostly caused by crystal stability and noise, which we deal with by temperature compensation, crystal aging or using higher tolerance crystals. This noise can be tracked by the receiving end, which is always equipped with some phase and frequency tracking capability. We must be more concerned with what can be called "short-term" noise. Short-term noise contains dynamic spectral characteristics that the receiver cannot deal with and thus becomes part of the communication system noise. Phase noise can also be viewed as a type of frequency modulation. When detected, there will be low and high frequency components. One can determine what threshold of FM noise can be tolerated simply by the communications application. In voice applications, frequency modulation less than 20 Hz is not audible so we can set our noise threshold at 20 Hz. Of course, if noise were to affect our communications system from a 1 Hz or even a 0.1 Hz offset, the requirements of signal purity would increase. The higher the signal purity, the more concentrated the signal energy is at the exact carrier frequency. In a statistical sense, a lower noise signal will have a lower standard deviation in frequency or phase perturbation.

Signal spectrum is (commonly) defined by its Single Side Band (SSB) noise density, the function L(fm). Note that since the noise spectrum is symmetrical around the vertical axis, the total noise is actually twice the single sided noise density. In the time domain, phase noise is expressed as jitter, and usually measured in radians, degrees, or seconds (psec) rms. FM theory provides an intuitive description of this effect. Suppose a signal is phase or frequency modulated by a sine-wave given by:

$$S(t)=\sin(\omega_0 t+m\sin(2\pi * fm * t)), \qquad \text{(Equation 27)}$$

where ω_0 is the carrier
fm is the modulating frequency
m is the index of modulation defined as the ratio between the maximum frequency deviation and fm, (m = dfmax / fm)

We know that the sideband (noise) power spectrum of such a signal is determined by Bessel functions and depends only on the index of modulation, m. When m is very small (< 0.1), the Bessel coefficients of higher order (>1) become negligible. Then the magnitudes of the two significant sideband spectral lines that appear around the carrier are m/2 (voltage) or $m^2/4$ (power) each.

We can calculate the jitter of the carrier ω_0 when corrupted by $m\sin(2\pi f_m t)$. Since m is the peak phase deviation level in radians, this will calculate to $m^2/2$ rad^2 rms jitter. Note that the total power of the two sidebands, (showing at offset of +/- fm from the carrier, each being $m^2/4$), is $m^2/2$. So without laborious math, we can infer that for small values of m, i.e. m < .1, the (integrated) power density of the noise is equal to its phase jitter in rad^2.

We can extend the argument from spectral lines to continuous spectral noise distribution with no loss of generality. The SSB phase noise density of the signal expressed by the function $L(f_m)$, is exactly what we measure on a spectrum analyzer when we watch the signal spectrum (see Figure 24). From this graph we can easily integrate the noise to determine the phase jitter.

Example:

A 1000 MHz signal is FM modulated by a 10 kHz signal with peak deviation of 300 Hz. We can calculate the spurious signal level and the jitter directly:

Let m = 300/10000 = 0.03

$S(t) = \sin(2\pi\omega_0 t + .03\sin(\omega_m t))$ has a jitter of +/- .03 radians peak. Therefore jitter is calculated as follows:

$\phi_N = .03/\sqrt{2} = .021$ rad rms

The signal spectrum will consist of a carrier (1000 MHz) and two sidebands, at +/- 10 kHz from the carrier, both with a relative level of:

$10\log(m^2/4) = -36.5$ dBC

Total sideband noise is -33.5 dBC = 20log(.021)

Thus we infer that for low m, the phase jitter can be calculated directly from the noise spectrum, phase noise or spurious signals.

Example:

If the carrier has 6 spurious signals at different offsets from the carrier, each at -40 dBC, we can calculate phase jitter as:

$\phi_N^2 = -40+10\log(6) = -32.2$ dBC.

Therefore the rms phase jitter will be:

$\phi_N = -32.2/2 = -16.1$dBC $\Rightarrow 10^{-1.61} = 0.0245$ rad or 1.4 degree rms.

Time jitter can be calculated from phase jitter as ϕ_N/ω_0. In this case $.0245/2\pi$ nsec = 3.89 psec. Thus the zero crossings of the signal, ideally exactly at 1000 psec interval, will have now a 3.89 psec rms jitter.

We have developed a method to derive time or phase jitter from the sideband or noise spectrum. This noise can be discrete (spurious) or distributed (phase noise) and the phase jitter will be given by the integral under the noise curve as follows:

$\phi_N = \sqrt{2}\int L(f_m)df$ rad rms or (Equation 28)
$\phi_N = 180\sqrt{2}\int L(f_m)df/\pi$ degrees rms
Tj (time jitter) $= \phi_N/\omega_0$ sec (Equation 29)

The multiplication by • 2 (Equation 28) is to account for the total noise energy (L(fm) is single sideband).

Remember that noise distribution or spurious are always relative to the carrier power. If the synthesizer has a noise distribution of -100 dBC/Hz at 10 kHz offset from the carrier, and if the carrier total power is +10 dBm, then this noise distribution is +10-100=-90 dBm/Hz at 10 kHz from the carrier.

Division and Multiplication Effect

One of the cardinal principles mentioned already, is that multiplication by N causes loss of 20log(N) in phase noise performance; division improves by the same number. If a 100 kHz crystal signal is multiplied by PLL (or any other way) to 1000 MHz, the multiplication ratio is 10,000 and the corruption in phase noise will be 80 dB.

When divided down by a digital divider, the divider improves jitter by N times or 20log(N) in noise power. The main reason for using fractional-N architecture, is to lower N, thus lowering the value of 20log(N).

Phase Noise Measurements

In the following, we will expand on practical calculations and measurements of phase noise parameters. Let's first estimate some practical numbers.

A North American cellular design that generates 900 MHz with a reference of 30 kHz (US cellular) has a multiplication N of 30,000 which calculates to 20log(30000)=90 dB. If the phase detector in a PLL has a noise density $L(f_m)$ that is flat, with level of -150 dBC/Hz, it will generate an output spectrum that, within the loop bandwidth, is corrupted by 90 dB. Thus, within the loop bandwidth, the effective PFD noise will be approximately -150 + 90 = -60 dBC/Hz. Such numbers can be measured directly on any synthesized spectrum analyzer. Other measurement methods include comparing (mixing) the signal to a better one in quadrature and measuring the resulting noise or by comparing the signals with its replica delayed (see Figure 28).

Sometimes FM noise is specified. This can be calculated (from offset f1 to f2, in Hz rms) by:

$$\delta f\ (\text{rms}) = \sqrt{2} \int fm^2\ (fm)\ dfm \quad \text{Hz} \qquad \text{(Equation 30)}$$

In the above example, this works out to 9.8 Hz rms (given: from 100 to 10KHz offset, loop bandwidth 600 Hz, using a micro-strip resonator VCO).

For an FM system with peak deviation of 2 kHz, the signal to noise ratio, (assuming both receive and transmit synthesizers are of same quality), caused by phase noise alone (with no additional channel noise) is: $20\log[(2000/9.8\sqrt{2})^2/2] \approx 40$ dB.

The Noise Distribution Function L(fm)

When the theory of phase noise started developing some 30 years ago, there were attempts to describe phase noise in phase variation, spectral representation and even in time domain. Time domain checks the signal time jitter, then calculates its noise spectrum. This is referred to as the Allan Variance. The measurement is complicated and requires high resolution and accurate computing counters. The industry eventually converged to spectral measurements, as every synthesizer designer has a spectrum analyzer. The function L(fm) is exactly the noise level seen on the spectrum analyzer, provided that the signal is not cleaner than the analyzer (in such case, we'll measure the analyzer phase noise). Typical good quality analyzers achieve phase noise better than -90 dBC/Hz at 100 Hz offset, -100 to -105 at 10KHz and -120 at 100 kHz offset. Most analyzers can not measure phase noise with 1 Hz bandwidth directly. The measurement has to subtract the resolution bandwidth (in dB) from the value.

Example:

Let offset = 5 kHz,
difference between center frequency and offset is 70 dB
resolution bandwidth is 100 Hz,

Then L(fm) will be approximately -70 - 20 = -90 dBC/Hz.

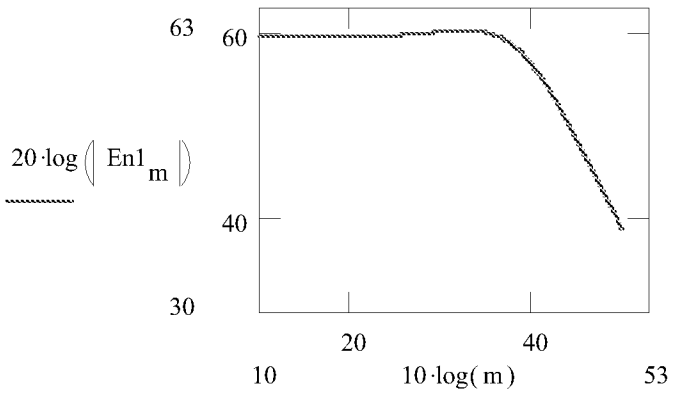
The analyzer has some correction factors that need be added, usually in the +/- 2 dB range. These emerge as a result of the type of detector in use (the spectrum analyzer detector is set to measure CW signals, noise measurement requires a correction factor) and bandwidth. Resolution noise bandwidth is not exactly that indicated by the instrument (a 100 Hz resolution filter can have 120 Hz noise bandwidth; this will cause 1 dB of measurement error).

Noise Sources in PLL

There are three cardinal noise sources in PLL circuits. Crystal oscillator phase noise affects performance very close to the carrier, usually below 10-100 Hz. Phase detector noise affects from 10-50 Hz to the loop bandwidth. Thereafter VCO noise becomes the dominant noise factor. The transfer functions for the crystal and the phase detector noises are very similar, and are given by the loop transfer function. Both will be multiplied by N within the loop bandwidth, and attenuated beyond (see Figure 23).

Note that the crystal reference Fr, usually derived from a crystal oscillator running at R * Fr, will be divided by R, thus gaining 20log(R) dB phase noise. A 30 kHz reference derived from a 9.6 MHz crystal gains 20log(9.6/.03)=50 dB. Even if the crystal phase noise at 10 Hz from carrier is only -100 dBC/Hz, after division it will be improved to –150 dBC/Hz, which is close to the phase detector noise. At higher offsets, the phase detector will have the dominant noise, with levels ranging from -135 to -165 dBC/Hz, depending on reference frequency and device in use. Phase detector noise increases with increasing Fr, at approximately 10 dB per decade rate. Both noises, crystal and phase detector, will be amplified by 20 log(N)dB within the loop bandwidth. Beyond loop bandwidth, (say >2ωn), they will be attenuated by the loop transfer function (see Figure 26) and the VCO noise will become dominant.

Figure 24. Crystal and Phase Detector Noise Transfer Function, N=1000



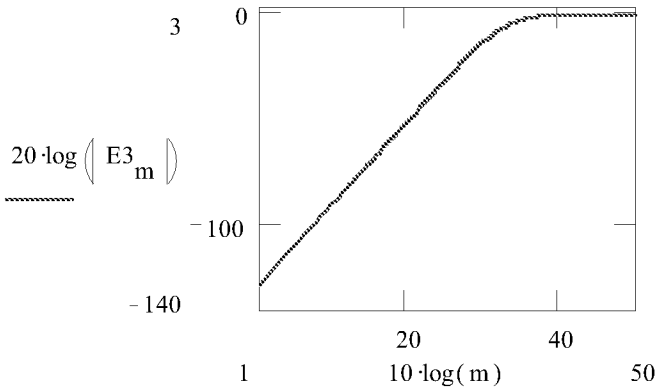
The VCO noise is multiplied by the transfer function:

$H_3(s) = s^2/(s^2+2s\xi\omega_n+ \omega_n^2)$

(VCO noise contribution will be composed of the VCO noise profile multiplied by this function).

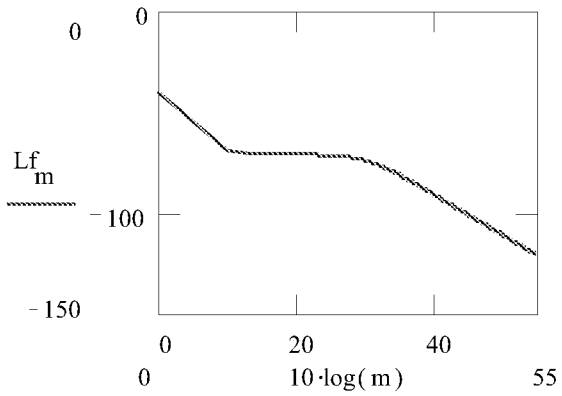
The transfer function that affects the VCO noise contribution $H_3(s)$, approaches unity for high offsets ($\omega > 2\omega_n$) but attenuates per $(\omega/\omega_n)^2$ for $\omega << \omega_n$. A simulation of VCO noise transfer function is shown in Figure 25. This is one of the more important features of PLL.

Figure 25. VCO Noise Transfer Function



While the VCO can be very noisy close to the carrier, this noise will be significantly attenuated within the loop bandwidth. Thus, for a VCO noise of -45 dBC/Hz at 100 Hz offset, the loop will contribute (in the case above) another 35 dB of attenuation, for a total of -80 dBC/Hz, significantly lower than the equivalent phase detector noise. Composite PLL phase noise is shown in Figure 26.

Figure 26. PLL Composite Phase Noise



The different noise sources show very clearly. Close to the carrier, the crystal is dominant, then from ≈ 50 Hz to the loop bandwidth, it's mainly the phase detector. At high offsets, ω>ωn, all other sources are attenuated and VCO noise controls the spectrum.

Spurious Suppression

Spurious signals are periodic interference, caused by radiation, power supply noise, mixing products, and reference (Fr) leakage. Reference signals generated in the phase detector (see Figure 8) modulate the VCO control line, causing spurious signals at the reference frequency Fr and its harmonics. There is a strict requirement on their suppression level as they interfere with the channel and corrupt adjacent spectra.

When multiplied by N, spurious signal levels increase by 20log(N) but their offset location from carrier stays the same. A 1 kHz spurious signal (say -100 dBC) on the reference (say 1 MHz), when multiplied by N=1000 times, will generate a 1 kHz offset spurious signal at the 1 GHz output frequency (with level -40 dBC).

Extra filtering is sometimes required to reduce spurious signal levels. This is the main reason for the common use of 3rd and 4th order loops.

Miniaturization of circuits puts a limit to the isolation between the digital circuits in the radio and RF sections, and some of the higher harmonics of the digital might leak, as might ground currents. Eliminating these effects requires expertise in circuit layout and grounding and shielding techniques. Detailed discussion of these issues is beyond the scope of this document.

Reference Spurious Signals

When in lock, the integer-N circuit's phase detector (being a digital part with limited speed) generates fast spikes that will leak and modulate the VCO control line, generating spurious signals at the reference frequency, Fr, and its harmonics. The spikes are short, usually in the 10nsec range, thus generating a spectrum of lines, Fr being the first and the hardest to filter. Harmonics of the line will also appear if not filtered sufficiently. Extra filtering (in most cases) is required for the 1st and 2nd harmonics. Higher harmonics are usually filtered out by the loop response.

Fractional Spurious Signals

In fractional-N circuits, because the compensation is not perfect, spurious signals will be generated at Fr and also at Fr/F and its harmonics. For Fr=480 kHz and F=16, the hardest spurious signal to filter will not be the reference F_r (which is quite high in frequency), rather it will be the 30 kHz spurious signal, (Fr/F, 480/16 = 30 kHz). Good fractional-N ASICs will compensate to -40 dBC or better. Additional filtering will be necessary. This is usually provided by the loop response. Also, the manufacturer may provide compensation adjustment. This may be manual, via a pin connected to potentiometer, or in software, to allow optimization in use. (The TI TRF2050 provides such a mechanism. See function CN on the chip). Fr is mostly attenuated by the 3rd order structure, providing significant extra filtering at the higher frequencies.

Spurious Signal Suppression

Few filtering techniques are needed to suppress spurious signals. In most cases a 3rd order loop is sufficient. If not, an extra R/C filter or sometimes two are added, and even notch filtering might be considered. These can be either LC type or twin-T structure.

External Filtering Techniques

The most common loop structure for cellular applications is the 3rd order loop shown in Figure 8. The capacitor C2 attenuates the current impulse spikes. Overall attenuation is achieved by the combination of the loop filter rejection and the external network. The attenuation level can be calculated by imposing the loop transfer function onto the impulse spectrum. Twin-T notch filters use resistor/capacitor components only and can be used as well. They will add 30-40 dB of attenuation.

Active Spurious Signal Cancellation

We have discussed so far two main methods for cancellation of spurious signals, one using filtering and one using feed forward current for fractional-N compensation. There is another fractional-N technology, (3rd order) using Sigma-Delta modulation approximation that is similar to the method used in audio CD players. This method enables spurious signal reduction via complex DSP operation, over sampling, and noise shaping. There are no such devices in the market at this time (early 1999), and the details of this method are beyond the scope of this document.

The Effect of Phase Noise on System Performance

Phase noise is a critical wireless issue because of its effect on the total communication system and network performance. Let us summarize the arguments we have raised so far in this document:

- Phase noise is part of the communication channel noise. Excess phase noise causes potential errors and adds to the channel noise.
- Channeling, accuracy and co-channeling are major considerations in wireless networks.
- Frequency re-use and low mutual interference is the basis for all cellular telephony.
- Spurious signals and excess phase noise can cause interference with other users.

- Spectral density and the scarcity of bandwidth force government regulators and communications designers to open up higher frequency bands (an example is the PCS band in response to the crowded cellular band.) At these higher frequencies, the phase noise requirements are more difficult to achieve mainly due to the higher multiplication ratios.

Loop Response Simulation

All loop response, transfer function, stability and spurious signal analysis can be accurately simulated. Most of the transfer functions and spurious signal rejection calculated in this document have been simulated on MATHCAD. Other math software as well as specific PLL software tools are available for design and analysis from COMPACT, HP, EAGLEWARE and others.

The EAGLEWARE software package has a comprehensive CAD tool designed specifically for PLL simulations.

Multi-Loop Design

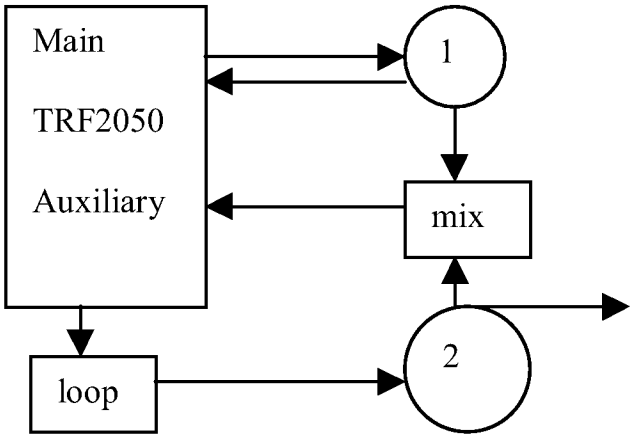
What alternatives are available for even lower phase noise? Sometimes the simple single loop design will not be sufficient even with fractional-N technology. In this event we must consider using multiple loops to reduce the division ratio.

Very complex schemes can be employed to reduce the division ratio resulting in very substantial phase noise improvement. It is possible, at least in theory, to design the circuit to perform at a noise level equal to the noise level of the multiplied crystal (at 1 GHz, loss of no more than 40 dB if the reference is 10 MHz). An example using the TI TRF 2052 is shown below (see Figure 27).

VCO1 is an auxiliary, using the main PLL section and a high reference frequency, say, 480 kHz. The loop can be wide, and we achieve excellent phase noise performance, some 15-20 dB better than with a lower reference. Then VCO2, the one used to generate the output frequency, is mixed down with VCO1 to generate a low frequency, say 9.6-10.05 MHz. The product then is connected to the Auxiliary input, where it is compared with Fr =30KHz to produce a 30 kHz step in the output. If VCO1 covers say, 960 (.48x2000) to 979.2 (.48x2040) MHz then the combined output will generate 969.6 to 989.25 MHz with 30 kHz step.

The division ratio of the main loop has been reduced to 2000 and the auxiliary loop to (320 - 335), significantly lower than a single loop (division will be in the 960/.03=32000 range). Phase noise improvement will be in the 20dB range. The price, of course, is an increase in complexity and cost. There are a variety of dual and multi-loop designs. This specific example is also referred to as “mix and count-down” architecture.

Figure 27. Mix and Count-Down Dual PLL



Measurements Techniques

We have already mentioned that some of the synthesizer parameters require special measurement techniques. We'll focus on phase noise, spurious signals and switching speed measurements.

Phase Noise

The easiest way to measure phase noise is to use a spectrum analyzer. In the case where the PLL circuit noise is lower than the analyzer's, there are alternative phase noise measurement systems. Comparing the Device Under Test (DUT) in quadrature to a low noise source (known to be much lower than the DUT) and calculating phase noise at the output of the mixer using an FFT analyzer is one method. Yet another way is to measure the phase of frequency error on a modulation analyzer.

A new set of instruments has emerged in the last few years which implement a frequency discriminator by mixing the signal with itself delayed (delay line of 200 nsec or so, using a coaxial cable). This method enables measuring free running VCO phase noise, but is limited to -45 dBC/Hz at 10 Hz offset. The measurement is a very quick and practical method for wireless applications (see Figure 28).

The simple math is as follows:
after the mixer,
$\sin(\omega t+\varphi(t))\sin(\omega(t+\tau+\phi)+\varphi(t+\tau))\Rightarrow \sin(\omega(\tau+\phi)+\varphi(t+\tau)-\varphi(t))$
where ϕ is just a phase shifter to bring the two signals to quadrature
$\varphi(t)$ is the noise, a random process with an average of 0 and some standard deviation.

Thus the calibrated output will be $\sin(\varphi(t)-\varphi(t+\tau)) \approx \tau(d\varphi/dt)$.

A more detailed analysis yields phase difference at phase detector given by:
$\delta\phi=\omega_0 t+\sin(\pi ft)\sin(2\pi f(t-\tau/2)2\delta f/f$,

and after approximations, the voltage at the output of the discriminator dV given by:
$dV=2\pi K\phi \bullet df \bullet \tau$ (for $f\tau << 1$) (Equation 31)
where: df is the offset from carrier,
$K\phi$ is the mixer constant.

Actually, the new constant, Kd, the frequency discriminator constant, can be expressed as:
$Kd=2\pi K\phi\tau$ and $\delta V=K*d\delta f$

At low offset, sensitivity is poor, thus the practical limitation of -45 dBC/Hz at 10 Hz offset.

Example, using a mixer with $K\phi$=0.1V/rad and τ=100 nsec, this calculates to:
Kd=0.06 μV/Hz and at 10 Hz offset, dV=0.6 μV/Hz.

Using a larger delay line (usually coax cable, not more than .5 μsec) will improve sensitivity, but the amount of improvement is limited.

Initially, the system is calibrated so that all gain stages, including phase detector loss are computed, Kd. Then the delayed carrier is brought to quadrature with the signal, and the product is processed on an FFT analyzer. Measurement is very fast, in the 5-10 second time frame.

Spurious Signals

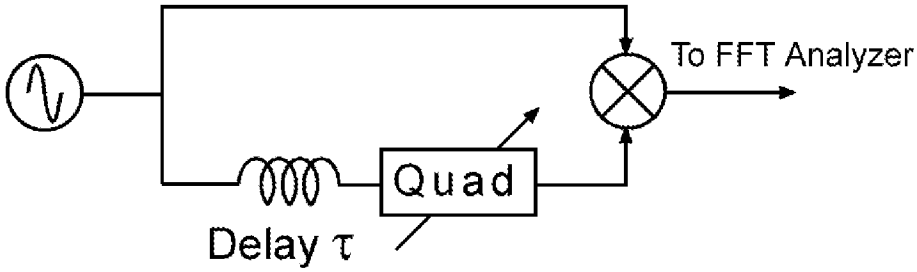
Spurious signal measurements are done directly on a Spectrum Analyzer. Any discrete line not related to the signal (excluding harmonics of the signal itself) is considered a spur. These include power supply noise (multiples of 60 Hz in North America and multiples of 50 Hz in Europe), reference Fr spurs (mainly 1st and 2nd harmonics), TCXO noise, Fx, as well as mixing products and any other spectral lines that might emerge as part of the radio design.

Switching Speed

There are few ways to measure speed:

- Use a modulation analyzer and set the measurement to be within a specified kHz from final frequency.
- Mix the hopping signal with a fixed reference set to the target frequency and check that the phase (in quadrature) is settled to within 0.1 radian or whatever the specification is.
- Use a pulse counter and check frequency after the specified speed (say 500 μsec).

Figure 28. Delay-Line Phase Noise Measurement



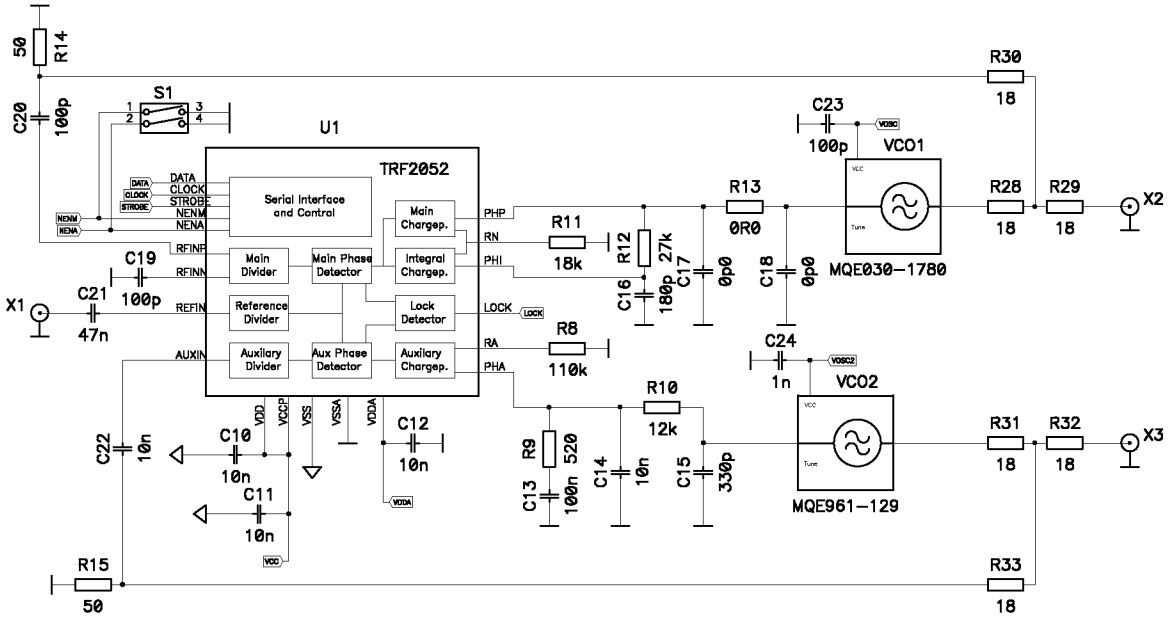
The TI Family of PLL ASICs

Texas Instruments is currently offering three PLL ASICs; two Integer-N types (TRF 2020, 2052), and one Fractional-N type (TRF 2050). The TRF2050 and TRF2052 are dual devices; they have a main and an auxiliary function, main to 1.2 GHz and auxiliary to 250 MHz. The TRF2020 is a triple device, main to 1.2 GHz and the auxiliaries to 250 MHz. One auxiliary was designed specifically for GSM internal clock generation.

For complete data sheets, please turn to our Web page. TI's Semiconductor Product Information Center at http://www.ti.com/cgi-bin/sc/support.cgi will assist you with your technical product inquiries. Our experts will provide you with accurate and prompt responses to your design-in and development needs.

Figure 29 shows the TRF2052 connected using both PLL functions and generating two signals used in wireless applications. The VCOs are from Murata (or Vari-L, Emheiser, Modco, Z-COM, and many others). Both loops use 4th order structure to attenuate the reference sidebands better.

Figure 29. Dual Synthesizer Using TRF2052



Summary and FAQ

PLL is a mature technology, yet continues to evolve rapidly. This document is a demonstration of TI's technical support and commitment to excellence in wireless technology. A second PLL document will be available dealing with design issues. Data sheets can be accessed on the Internet and evaluation boards are available from TI, including complete hardware and control software. The new PLL chips from TI represent a new dimension in functionality, density and performance. PLL circuits require an external crystal, VCO and loop filter; otherwise, all functions are performed internally.

All signals are narrow band noise. Noise shape can be controlled by loop parameters but within the loop bandwidth, will be corrupted by 20log(N).

A better noise spectrum can be achieved by lowering N. This can be done by either using fractional-N architecture or multi-loop designs.

The most popular PLL structure for wireless applications is the 3rd order loop, for which the following equations apply (see Figure 8):
$\omega n=(KvK\phi/NC1)^{0.5}$
$\xi=R/2(N/KvK\phi C1)^{2}$

Tsw, switching time to df for a dF excursion, is given by:
$Tsw = -\ln(\xi df/dF)/\xi\omega n$

For these equations, Kv is in rad/secV, and $K\phi$ is in A/rad

Detailed data sheets, application notes, evaluation cards and tech briefs, along with staff support, is available from Texas Instruments at TI's Semiconductor Product Information Center, on the Web at http://www.ti.com/cgi-bin/sc/support.cgi.

Some of the FAQs:

How do I further attenuate reference spurious signals?
Additional filtering can be achieved by adding R/C or notch filters. Loop stability must be calculated and phase margin should be at least 40 degrees.

How can I improve my phase noise performance?
The best approach is to start to use fractional-N technology and reduce the division ratio.

Why does phase noise lose 20logN within the loop bandwidth?
Because PLLs operate as a frequency multiplier by N.

How much performance do we lose due to the fact that phase error is measured only at zero crossings?
Almost none. All timing information is contained in the zero crossings.

How do we calculate phase jitter from phase noise?
You must use a computer program; it involves an integration process. See the PHAZNOIZ program, available from Texas Instruments.

What speed improvement can we expect from speed up?
Up to ratio of 10:1.

Why does lowering loop bandwidth reduce phase noise performance?
Usually, for low loop bandwidth, the VCO noise rejection is poor. Close to the carrier, this will add, and corrupt overall phase noise performance.

Glossary

AM	amplitude modulation
AMPS	Advanced Mobile Phone Service/System
dB	decibel
dBC/Hz	power relative to total signal power
dBm	decibel relative to 1 mW (1mW = 0 dBm)
Er	error, noise
f_m, ω_m	modulating frequency
F	fractionality, noise figure
FM	frequency modulation
Fr	reference frequency
Fo	VCO output frequency
Fx	crystal frequency
F(s), H(s)	transfer function
GCD(x,y)	greatest common divisor
Kv	VCO constant, usually in MHz/Volt
Kd	phase detector constant, usually V/rad or mA/rad
L(fm)	single sideband noise density
LD	lock detect
LSB	list significant bit
M, A, N	PLL counters
MSB	most significant bit
m	index of modulation
MC	modulus control
N	division ratio
P	dual modulus basic divider
PFD	phase frequency detector
R	crystal divider
PM	phase modulation
SSB	single side band

VCO	Voltage Controlled Oscillator
T, t, τ	time or time delay
TCXO	Temperature Compensated Crystal Oscillator
ξ	damping factor
ϕ, φ	phase
ϕ_M	phase margin
ωn	natural frequency
ω_0	center or carrier frequency
ωp	frequency where open loop gain equals 1

References and Further Reading

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